# S1C17M01



### Flow meter controller with AFE

### **■ DESCRIPTIONS**

The S1C17M01 is an ultra low-power MCU equipped with an MR (magneto resistive) sensor controller that allows an MR sensor array optimized for flow measurement (recommended sensor: KG1205-61 manufactured by KOHDEN Co., Ltd.) to be connected directly. This IC includes an LCD driver to display the flow count and the readouts on the indicator, and the synchronous serial interface, UART, and I2C interface for wireless communication with a remote meter reading system. This IC allows measurement of various environmental conditions such as a temperature and humidity measurement using the R/F converter, and a supply voltage measurement using the supply voltage detection circuit.

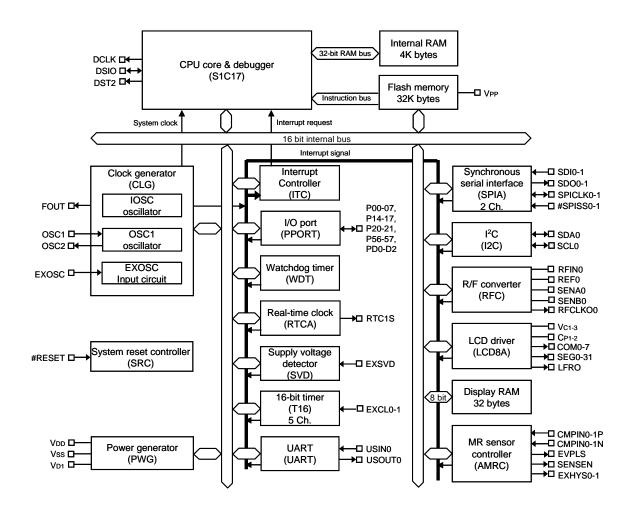
### **■ FEATURES**

Model	S1C17M01
CPU	
CPU core	Seiko Epson original 16-bit RISC CPU core S1C17
Other	On-chip debugger
Embedded Flash memory	
Capacity	32K bytes (for both instructions and data)
Erase/program count	50 times (min.) *Programming by the debugging tool ICDmini
Other	Security function to protect from reading/programming by ICDmini
	On-board programming function using ICDmini
Embedded RAM	The state programming random asing roomining
Capacity	4K bytes
Embedded display RAM	
Capacity	32 bytes
Clock generator (CLG)	V= x)
System clock source	3 sources (IOSC/OSC1/EXOSC)
System clock frequency	16.3 MHz (max.)
(Operating frequency)	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
IOSC oscillator circuit	7.37 MHz (typ.) embedded oscillator
(boot clock source)	5 us (max.) starting time (time from cancelation of SLEEP state to vector table read by the
(==== 5.00 000.00)	CPU)
OSC1 oscillator circuit	32.768 kHz(typ.) crystal oscillator
	Oscillation stop detection circuit included
EXOSC clock input	16.3 MHz (max.) square or sine wave input
Other	Configurable system clock division ratio
	Configurable system clock used at wake up from SLEEP state
	Operating clock frequency for the CPU and all peripheral circuits is selectable.
I/O port (PPORT)	
Number of general-purpose I/O ports	19 bits (max.) (Pins are shared with the peripheral I/O.)
Number of input interrupt ports	8 bits
Timers	
Watchdog timer (WDT)	Generates NMI or watchdog timer reset.
Real-time clock (RTCA)	128 – 1 Hz counter, second/minute/hour/day/day of the week/month/year counters
	Theoretical regulation function for 1-second correction
	Alarm and stopwatch functions
16-bit timer (T16)	5 channels
	2 channels can generate the SPIA master clock.
Supply voltage detection circuit (SVD)	
Detection level	20 levels (1.8 to 3.7 V)
Other	Intermittent operation mode
	Generates an interrupt or hardware reset according to the detection level evaluation.
Serial interfaces	
UART (UART)	1 channel
	Baud-rate generator included, IrDA1.0 supported
Synchronous Serial Interface (SPIA)	2 channels
	The 16-bit timer (T16) can be used for the baud-rate generator in master mode.
I <sup>2</sup> C (I2C)	1 channel
	Baud-rate generator included
LCD driver (LCD8A)	
LCD output	32 SEG x 1 to 4 COM (max.), 28 SEG x 5 to 8 COM (max.)
LCD dulput	32 0E 6 X 1 to 4 00M (Max.), 20 0E 6 X 3 to 0 00M (Max.)

## S1C17M01

Other	1/3 bias power supply included, external voltage can be applied.
R/F converter (RFC)	
Conversion method	CR oscillation type with 24-bit counters
Number of conversion channels	1 channel (Up to two sensors can be connected.)
Supported sensors	DC-bias resistive sensors and AC-bias resistive sensors
MR sensor controller (AMRC)	
MR sensor interface	MR sensor is directly connectable.
Measurement functions	Evaluates normal rotation, reverse rotation, stop, and phase dropout by inputting
	analog rotation phase signals from an MR sensor.
External interface	Pulse output function
	External hysteresis resistor control function
Reset	
#RESET pin	Reset when the reset pin is set to low.
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).
Supply voltage detection circuit reset	Reset when SVD detects the set voltage level (can be enabled/disabled using a register).
Interrupt	
Non-maskable interrupt	4 systems (Reset, address misaligned interrupt, debug, NMI)
Programmable interrupt	External interrupt: 1 system (8 levels)
•	Internal interrupt: 15 systems (8 levels)
Power supply voltage	
VDD operating voltage	1.8 to 5.5 V
VDD operating voltage when AMRC is active	2.0 to 5.5 V
VDD operating voltage for Flash	1.8 to 5.5 V (VPP = 7.5 V external power supply is required.)
programming	
Operating temperature	
Operating temperature range	-40 to 85 °C
Current consumption	
SLEEP mode	0.35 uA
	IOSC = OFF, OSC1 = OFF, VDD = 3.6 V
HALT mode	0.8 uA
	IOSC = OFF, OSC1 = 32 kHz, RTC = ON, VDD = 3.6 V
	1.3 uA
	IOSC = OFF, OSC1 = 32 kHz, RTC = ON, CPU = OSC1, LCD = ON (no panel load, Vc2
	reference)
RUN mode	12.5 uA
	IOSC = OFF, OSC1 = 32 kHz, RTC = ON, CPU = OSC1, LCD = ON (no panel load, Vc2
	reference)
	2.5 mA @ 1/1 divided clock
	IOSC = ON, OSC1 = 32 kHz, RTC = ON, CPU = IOSC, LCD = OFF (no panel load)
	500 uA @ 1/4 divided clock
	IOSC = ON, OSC1 = 32 kHz, RTC = ON, CPU = IOSC, LCD = OFF (no panel load)
Shipping form	
1	TQFP13-64pin (Lead pitch: 0.5 mm)
2	Die form (Pad pitch:100 um)

### **■ BLOCK DIAGRAM**



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MICRODEVICES OPERATIONS DIVISION

EPSON semiconductor website

http://www.epson.jp/device/semicon\_e/

IC Sales & Marketing Department

421-8 Hino, Hino-shi, Tokyo 191-8501, JAPAN Phone: +81-42-587-5814 FAX: +81-42-587-5117

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