

OVERVIEW

The SM8220/SM8221 Calling Number Identification Receiver IC is a CMOS integrated circuit, which provides an interface to various calling information delivery services such as Calling Number Delivery (CND) and Calling

Name Delivery (CNAM) compatible with the Bellcore GR-30-CORE. The device also contains a power down circuit, a ring detect circuit and a carrier detect circuit for easier system implementation.

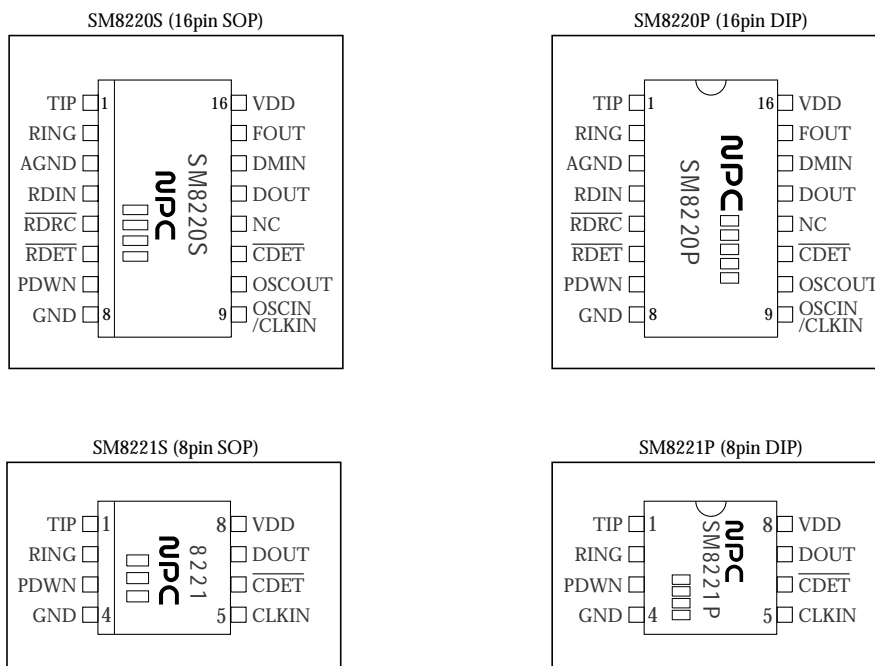
FEATURES

- Compatible with Bellcore GR-30-CORE
- Integrated band pass filter
- FSK demodulator
 - Bell 202 and ITU-T V.23
- High input sensitivity: -48 dBm typical
- Ring detect output
- Carrier Detect Output (SM8220)
- Power down mode: 1μA power down current
- Uses 3.579545 MHz crystal (SM8220) or external clock source
- Power supply voltage: 3V to 5.5V
- Low power consumption
- Molybdenum-gate CMOS process
- Package
 - SM8220: 16 pin SOP, 16 pin DIP
 - SM8221: 8 pin SOP, 8 pin DIP

APPLICATIONS

- Calling Number Delivery service
- Adjunct Boxes
- Telephone Answering Machines
- Feature Phones
- Fax Machines
- Computer Interface Products

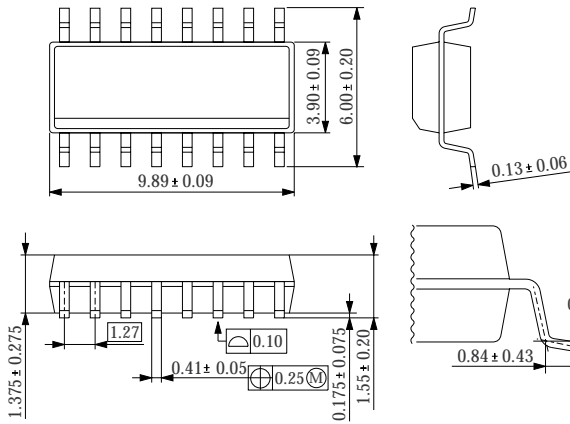
PINOUT (Top View)



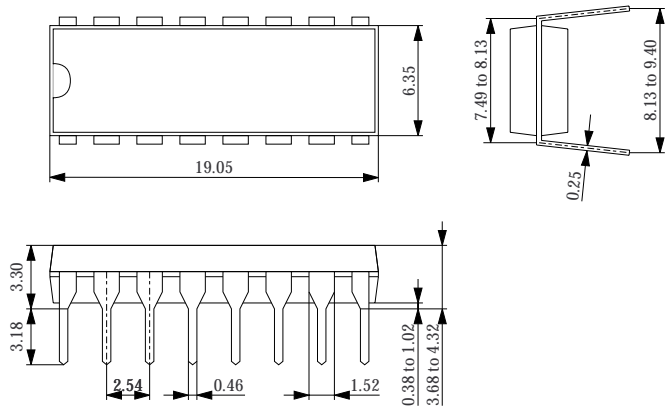
SM8220/SM8221

PACKAGE DIMENSIONS (Unit: mm)

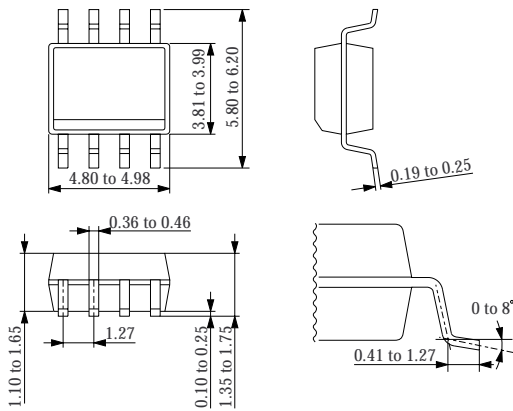
SM8220S (16 pin SOP)



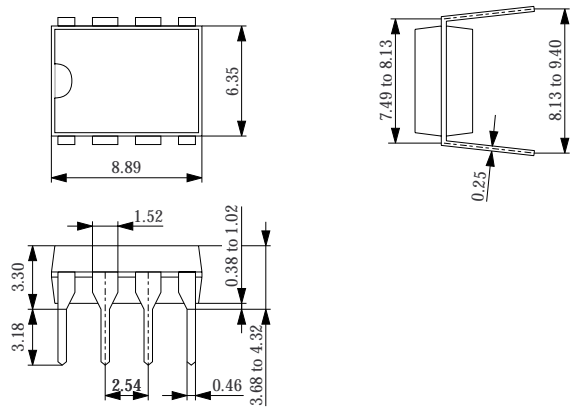
SM8220P (16 pin DIP)



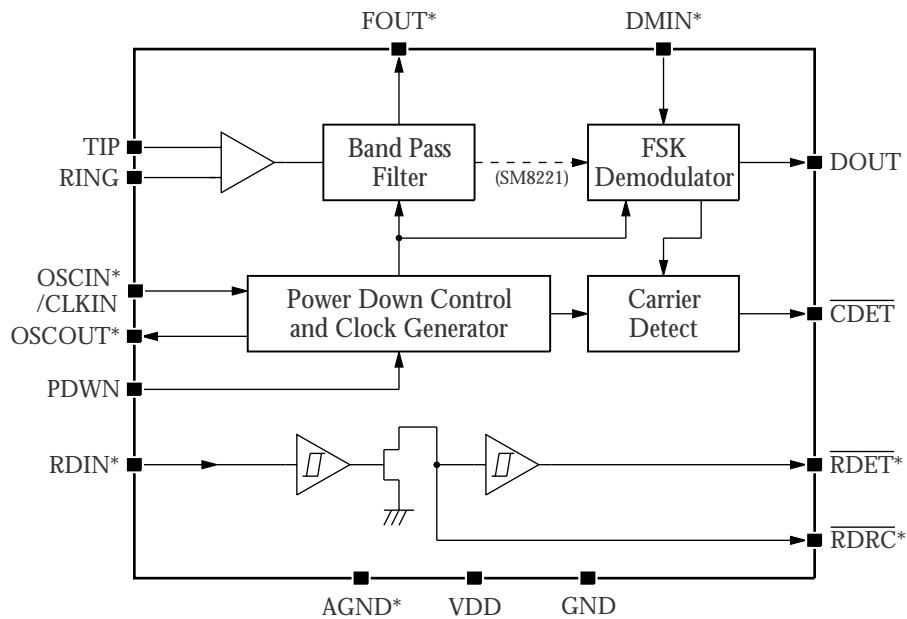
SM8221S (8 pin SOP)



SM8221P (8 pin DIP)



BLOCK DIAGRAM



*: Not available for SM8221.

SM8220/SM8221

PIN DESCRIPTIONS

Number		Name	i/o	Function
SM8220	SM8221			
1	1	TIP	i	Tip Input: This pin is connected to the tip side of the twisted pair telephone wires. This pin must be DC isolated from the phone line.
2	2	RING	i	Ring Input: This pin is connected to the ring side of the twisted pair telephone wires. This pin must be DC isolated from the phone line.
3	-	AGND	o	Analog Ground: 1/2 V _{DD} voltage output. This pin must be grounded through 0.1 μF capacitor.
4	-	RDIN	si	Ring Detect Input: The attenuated ring signal is connected to this pin for the ring detection.
5	-	$\overline{\text{RDRC}}$	od	Ring Detect RC Terminal: An RC network will be connected to this pin to set time delays for the ring signal detection.
6	-	$\overline{\text{RDET}}$	o	Ring Detect Output: This pin is an output of a schmitt trigger buffer which input is connected to $\overline{\text{RDRC}}$ pin. The low level at this pin indicates that the ring signal is detected.
7	3	PDWN	si	Power Down Control: This pin must be kept at low level for the normal operation. When it is high, the device will be in the power down. Under the power down mode, OSCOUT, $\overline{\text{CDET}}$ and DOUT pins are set to high level and AGND, FOUT pins are set to high impedance.
8	4	GND	-	Device Ground: This pin is connected to the system ground.
9	5	OSCIN /CLKIN	i	Crystal Oscillator Input: A crystal will be connected between this pin and OSCOUT pin. This pin may be driven from an external clock source.
10	-	OSCOUT	o	Crystal Oscillator Output: A crystal will be connected between this pin and OSCIN pin. This pin must be kept open when OSCIN pin is driven from an external clock source.
11	6	$\overline{\text{CDET}}$	o	Carrier Detect Output: When low, this output indicates that a valid carrier present on the line.
12	-	NC	-	No connection pin.
13	7	DOUT	o	Data Out: This pin presents the output of the demodulator while $\overline{\text{CDET}}$ pin is low. When $\overline{\text{CDET}}$ pin goes high, this pin is held high.
14	-	DMIN	i	Demodulator Input: This pin is connected from FOUT pin through a 0.1μF capacitor. No other components should be connected to this pin.
15	-	FOUT	o	Band Pass Filter Output: This pin is connected to DMIN pin through a 0.1μF capacitor. No other components should be connected to this pin.
16	8	VDD	-	Power Supply: Positive power supply pin.

(Note) si: Schmitt Triger Input, od: Open Drain Output.

SM8220/SM8221

ABSOLUTE MAXIMUM RATINGS

(GND= 0V unless otherwise noted)

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V _{DD}		-0.5 to 7.0	V
Input Voltage	V _{IN}		-0.3 to V _{DD} +0.3	V
Input Current	I _{IN}		±10	mA
Power Dissipation	P _D		120	mW
Operating Temperature Range	T _a		-20 to 85	°C
Storage Temperature Range	T _{STG}		-40 to 125	°C
Soldering Temperature	T _{SLD}		255	°C
Soldering Time	t _{SLD}		10	sec

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(V_{DD}= 5±0.5 V, GND = 0 V, f_{CLK} = 3.579545 MHz, T_a = -20 to 85 °C unless otherwise noted)

Parameter	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
DC Supply Voltage	V _{DD}		3	5	5.5	V
Supply Current	I _{DD}	*1		1.7	3	mA
Power Down Current	I _{DPD}	*2			1	μA
Input Low Voltage1	V _{IL1}	OSCIN/CLKIN pin V _{OSCOUT} = 0.8V _{DD}			0.3V _{DD}	V
Input High Voltage1	V _{IH1}	OSCIN/CLKIN pin V _{OSCOUT} = 0.2V _{DD}	0.7V _{DD}			V
Input Low Voltage2	V _{IL2}	PDWN, RDIN, $\overline{\text{RDRC}}$ pin		2	0.3V _{DD}	V
Input High Voltage2	V _{IH2}	PDWN, RDIN, $\overline{\text{RDRC}}$ pin	0.75V _{DD}	3		V
Output Low Voltage	V _{OL}	DOUT, $\overline{\text{RDET}}$, $\overline{\text{CDET}}$, $\overline{\text{RDRC}}$ pin, V _{DD} = 4.5V, I _{OL} = 1.6mA			0.4	V
Output High Voltage	V _{OH}	DOUT, $\overline{\text{RDET}}$, $\overline{\text{CDET}}$ pin V _{DD} = 4.5V, I _{OH} = -1.6mA	3.7			V
Input Leakage Current	I _{IN}	OSCIN/CLKIN, PDWN, RDIN pin, V _{DD} = 5.5V, V _{IN} = 0 or 5V	-1		1	μA
Output Leakage Current	I _{OFF}	$\overline{\text{RDRC}}$ pin, RDIN= 0V V _{DD} = 5.5V, V _{OH} = 5.5V			1	μA
Input DC Resistance	R _{IN}	TIP, RING pin, V _{DD} = 5V Impedance measured from 1/2V _{DD}	175	250	325	kΩ

*1: OSCIN/CLKIN= 0V, PDWN= 0V, RDIN= 0V, $\overline{\text{RDRC}}$ = 0V, Other Input Pins= open

*2: OSCIN/CLKIN= 0V, PDWN= V_{DD}, RDIN= 0V, $\overline{\text{RDRC}}$ = 0V, Other Input Pins= open

SM8220/SM8221

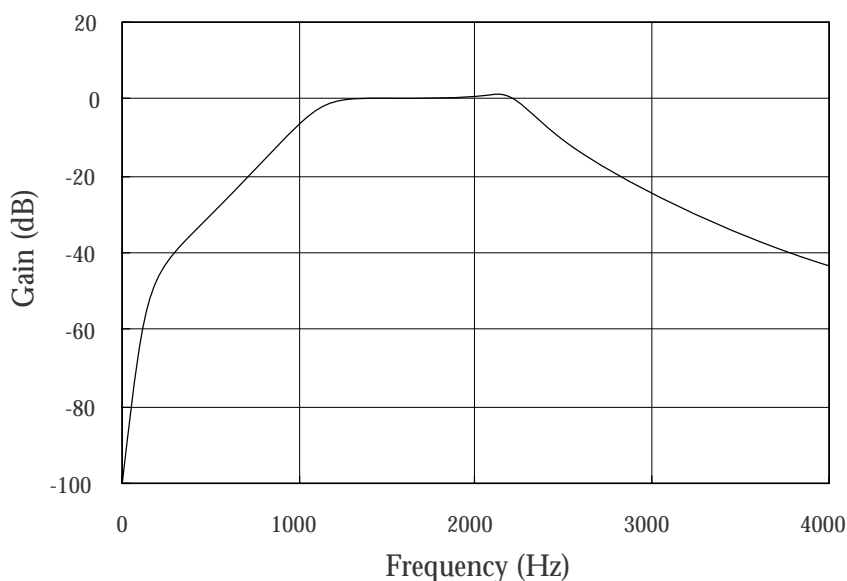
AC CHARACTERISTICS

($V_{DD}=5.0V$, $GND=0V$, $f_{CLK}=3.579545MHz$, $T_a=-20$ to $85\text{ }^\circ C$, $0dBm=0.7746V_{rms}$ @ 600Ω unless otherwise noted)

Parameter	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Input Sensitivity		TIP, RING pin		-48		dBm
TIP, RING pin Input Level		$V_{DD}=5V$			-15	dBm
		$V_{DD}=3V$			-18	
Band Pass Filter Frequency Response (relative to 1700 Hz @ -34 dBm input level)		60Hz		-80		dB
		1200 Hz		-1		
		2200Hz		0		
		4000Hz		-43		
		$\geq 10000Hz$		-54		
Carrier Detect ON Sensitivity	CD_{ON}	\overline{CDET} pin		-48	-44	dBm
Carrier Detect OFF Sensitivity	CD_{OFF}	\overline{CDET} pin	-55	-51		dBm
Oscillator Frequency	f_{CLK}		-0.1%	3.579545	+0.1%	MHz

TYPICAL BAND-PASS FILTER FREQUENCY RESPONSE

(Relative to 1700 Hz @ -34 dBm input level)



SWITCHING CHARACTERISTICS

($V_{DD}=5.0V$, $GND=0V$, $f_{CLK}=3.579545MHz$, $T_a=25\text{ }^\circ C$, $C_L=50pF$ unless otherwise noted)

Parameter	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Power Down Low to Oscillator Start Up	t_{DOSC}			5		ms
Power Down Low to FSK Data Detect	t_{SUPD}			10		ms
Carrier Detect Acquisition Time	t_{DAQ}			10		ms
End of Data to Carrier Detect High	t_{DCH}			10		ms

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FUNCTIONAL DESCRIPTION

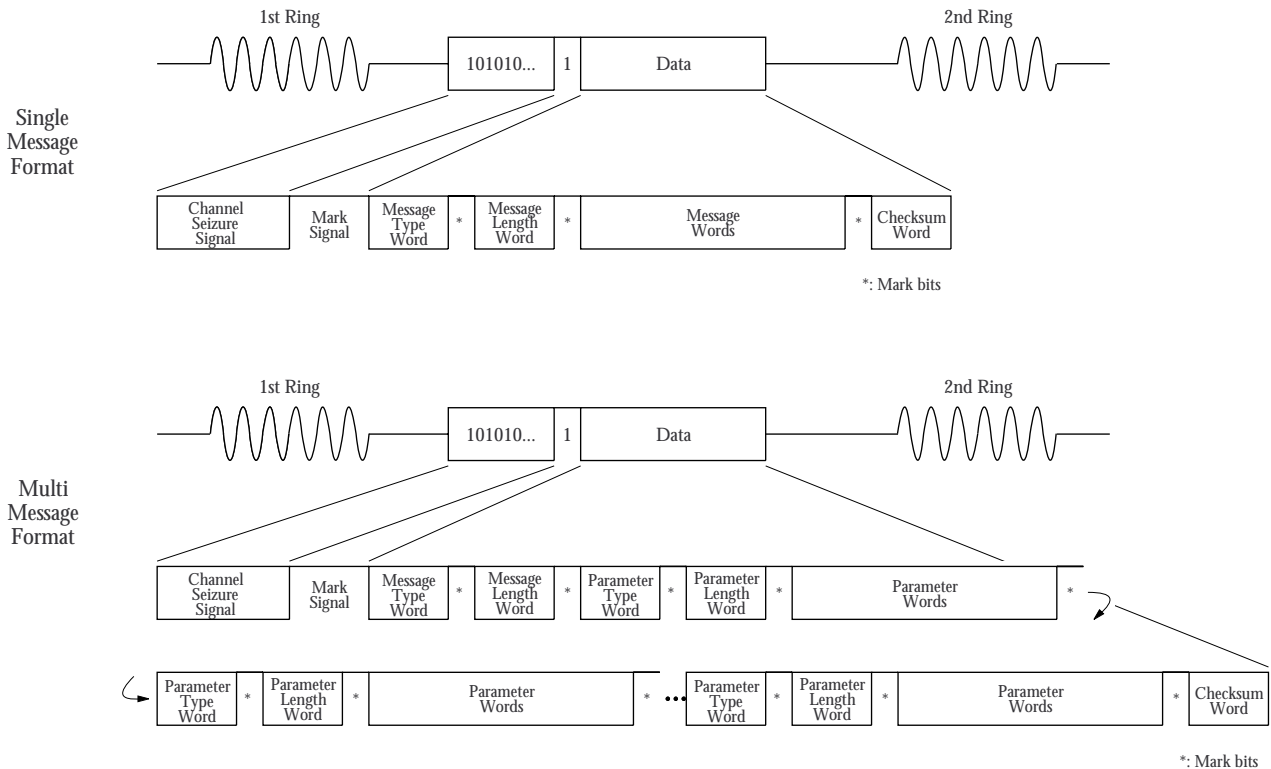
The SM8220/SM8221 Calling Number Identification Receiver IC is a device compatible with the Bellcore GR-30-CORE for transmitting asynchronous voice-band data to Customer Premises Equipment (CPE) from a serving Stored Program Controlled Switching System (SPCS) or a Central Office (CO). This data transmission technique is

applicable in a variety of services such as Calling Number Delivery (CND), Calling Name Delivery (CNAM). With these services, a subscriber will have the ability to display a message containing the phone number of the calling party, the name of a calling party, the date and the time.

The data signaling interface should conform to Bell 202 and ITU-T V.23 specification, which is:

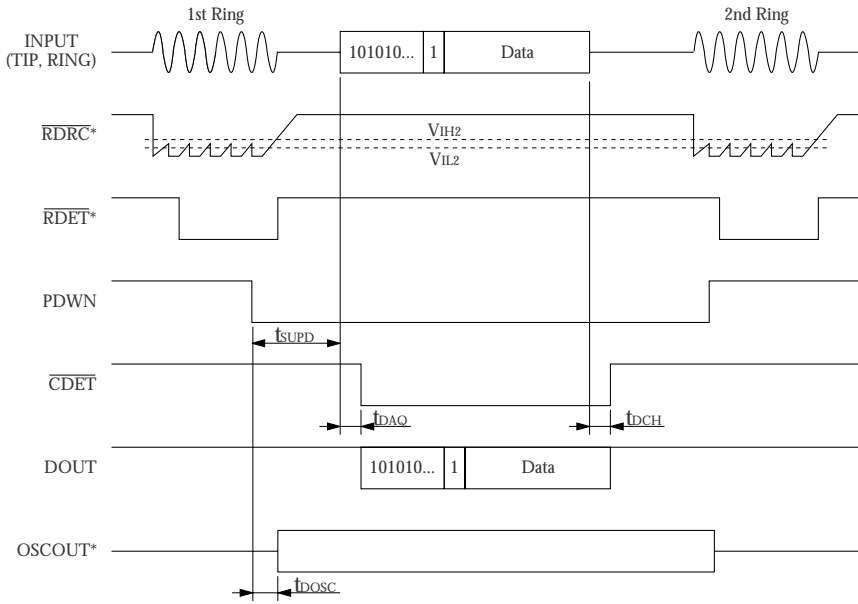
	Bell 202	ITU-T V.23
Modulation Type	Continuous - phase binary frequency shift keying (FSK)	
Logical 1 (Mark)	1200 ± 12Hz	1300 ± 22Hz
Logical 0 (Space)	2200 ± 22Hz	2100 ± 22Hz
Carrier Frequency	1700Hz	1700Hz
Transmission rate	1200BPS	1200BPS
Data format	serial, asynchronous	serial, asynchronous

Bellcore GR-30-CORE Data Format



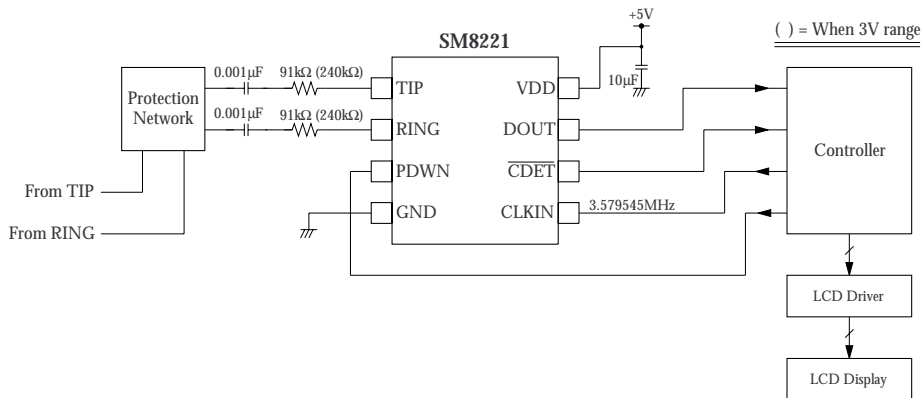
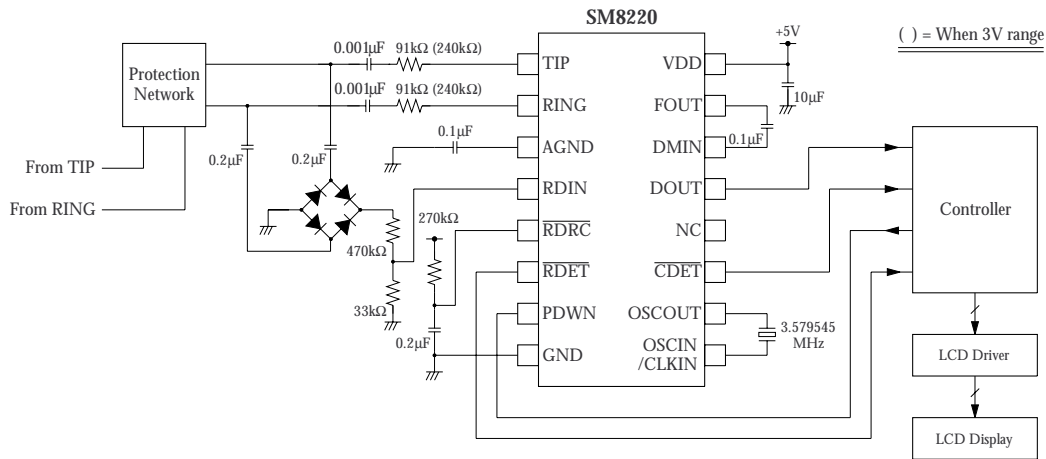
SM8220/SM8221

TIMING DIAGRAM



*: Not available for SM8221.

TYPICAL APPLICATION CIRCUIT



(Note)

When the Ring Detect feature of SM8220 is not used, always connect **RDIN** and **RDRC** pins to the system ground level. This will cut excess current drain from **VDD** under the normal and power down mode of operation. This diagram example is designed to adapt to the specifications of United States. When it is used in other area, the constants may have to be changed appropriately.

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