RoHS

RF Power LDMOS Transistors

N–Channel Enhancement–Mode Lateral MOSFETs

AFT21S230SR3
AFT21S230–12SR3
AFT21S232SR3

2110–2170 MHz, 50 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTORS

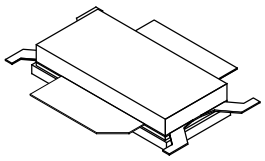
These 50 W RF power LDMOS transistors are designed for cellular base station applications covering the frequency range of 2110 to 2170 MHz.

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 1500 mA, P_{out} = 50 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

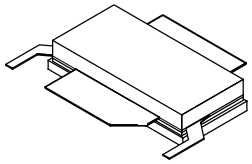
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	16.7	30.5	7.2	–35.7	–19
2140 MHz	17.0	31.0	7.1	–35.4	–20
2170 MHz	17.2	31.8	7.0	–34.8	–15

Features

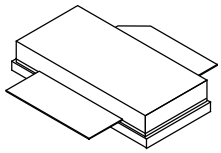
- Greater Negative Gate–Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- NI–780S–2L2L, NI–780S–2L4S: R3 Suffix = 250 Units, 44 mm Tape Width, 13–inch Reel.
- NI–780S–2L: R3 Suffix = 250 Units, 56 mm Tape Width, 13–inch Reel.
For R5 Tape and Reel options, see p. 17.



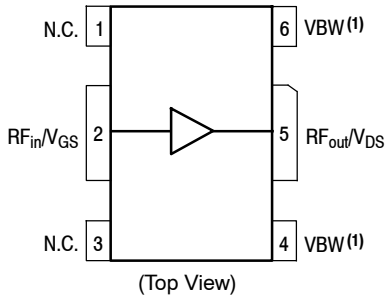
NI–780S–2L4S
AFT21S230SR3



NI–780S–2L2L
AFT21S230–12SR3

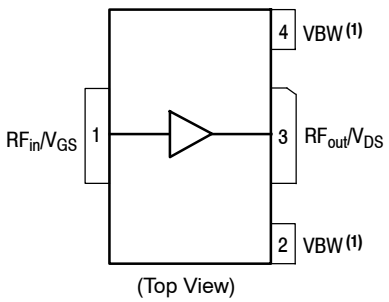


NI–780S–2L
AFT21S232SR3



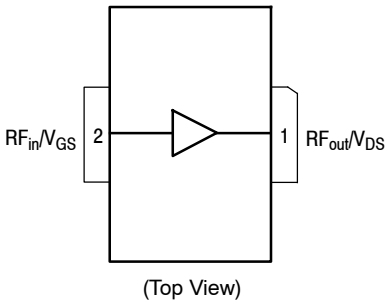
(Top View)

Figure 1. Pin Connections



(Top View)

Figure 2. Pin Connections



(Top View)

Figure 3. Pin Connections

1. Device can operate with the V_{DD} current supplied through pin 4 and pin 6 (AFT21S230S) or pin 2 and pin 4 (AFT21S230–12S) at a reduced RF output power level. Refer to CW operation data in the Maximum Ratings table.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C
CW Operation @ T_C = 25°C when DC current is fed through drain lead, pin 5 (AFT21S230S), pin 3 (AFT21S230-12S) or pin 1 (AFT21S232S) Derate above 25°C	CW	 161 0.75	 W W/°C
CW Operation @ T_C = 25°C when DC current is fed through pin 4 and pin 6 (AFT21S230S) or pin 2 and pin 4 (AFT21S230-12S) Derate above 25°C	CW	 104 0.44	 W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 50 W CW, 28 Vdc, I_{DQ} = 1500 mA, 2110 MHz Case Temperature 86°C, 140 W CW (4), 28 Vdc, I_{DQ} = 1500 mA, 2110 MHz	$R_{\theta JC}$	 0.43 0.38	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 291 μAdc)	$V_{GS(th)}$	1.5	2.0	2.5	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1500 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.2	2.7	3.2	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3.7 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

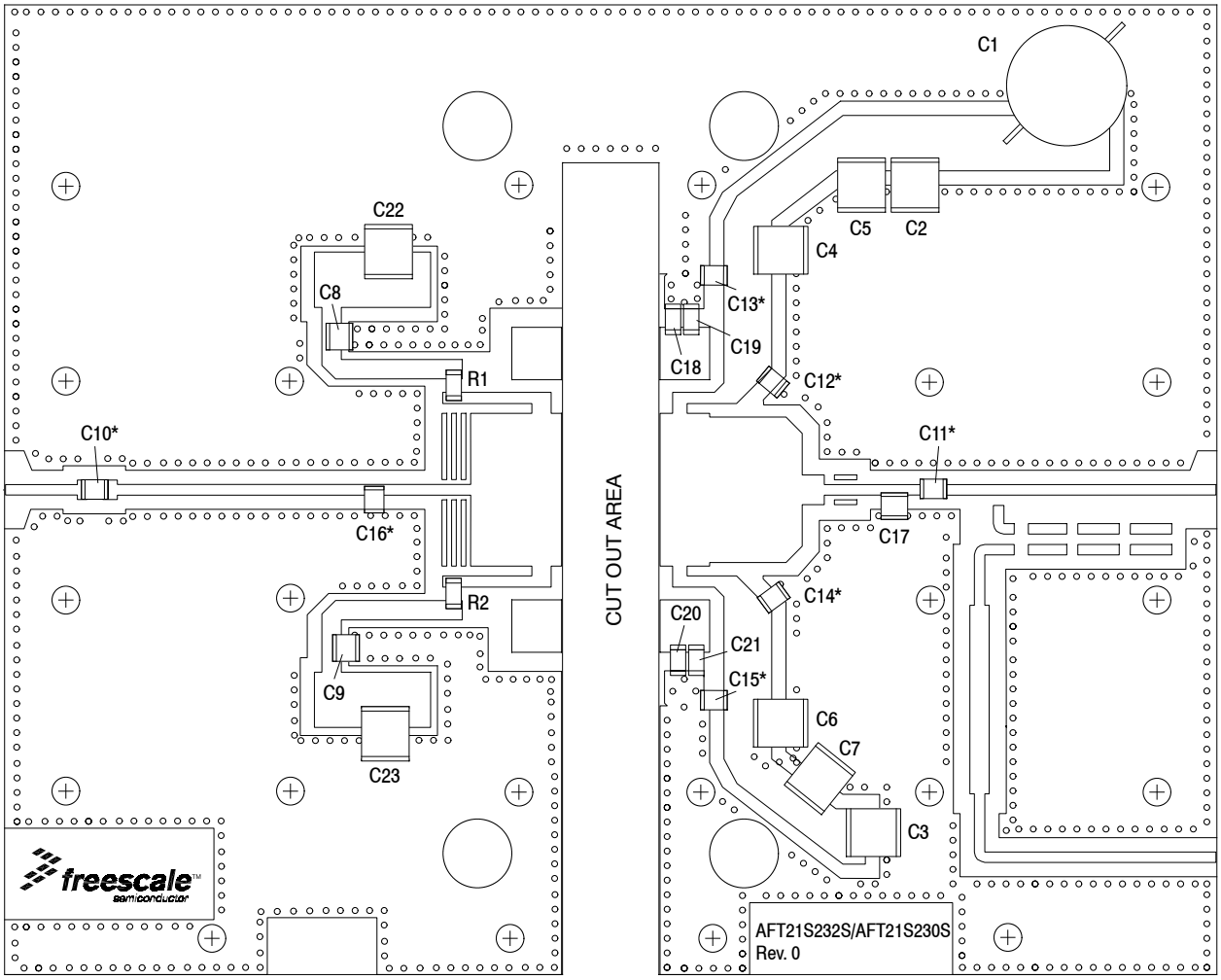
1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1500 mA, P_{out} = 50 W Avg., f = 2110 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	16.0	16.7	19.0	dB
Drain Efficiency	η_D	29.0	30.5	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.7	7.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	-35.7	-34.0	dBc
Input Return Loss	IRL	—	-19	-10	dB
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 1500 mA, f = 2140 MHz					
VSWR 10:1 at 32 Vdc, 269 W CW (2) Output Power (3 dB Input Overdrive from 182 W CW (2) Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1500 mA, 2110-2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	182 (2)	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110-2170 MHz bandwidth)	Φ	—	-19.3	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point) AFT21S230S AFT21S232S	VBW_{res}	—	 95 60	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 50 W Avg.	G_F	—	0.5	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.016	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C) (2)	ΔP1dB	—	0.007	—	dB/°C

1. Part internally matched both on input and output.
2. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.



*C10, C11, C12, C13, C14, C15 and C16 are mounted vertically.

Figure 4. AFT21S230SR3(232SR3) Test Circuit Component Layout

Table 5. AFT21S230SR3(232SR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	470 μF, 63 V Electrolytic Capacitor	B41694A5477Q7	EPCOS
C2, C3, C4, C5, C6, C7, C22, C23	10 μF, 100 V Chip Capacitors	C5750X7S2A106M	TDK
C8, C9, C10, C11, C12, C13, C14, C15	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C16	0.6 pF Chip Capacitor	ATC100B0R6BT500XT	ATC
C17	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C18, C19, C20, C21	1 μF, 50 V Chip Capacitors	CDR34BX104AKWS	AVX
R1, R2	8.2 Ω, 1/4 W Chip Resistors	RC1206FR-108R2L	Yageo
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	—	MTL

TYPICAL CHARACTERISTICS

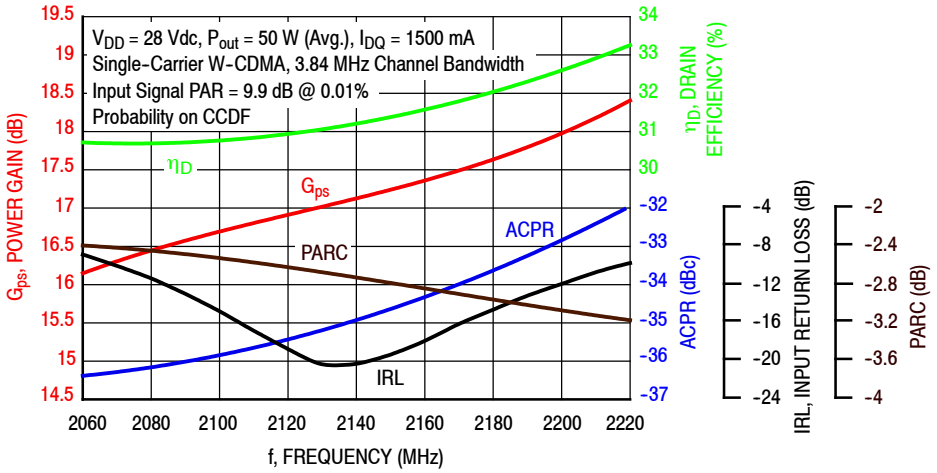


Figure 5. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 50 Watts Avg.

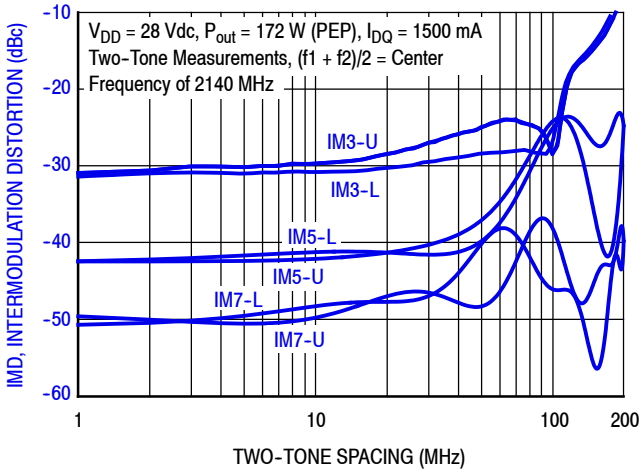


Figure 6a. Intermodulation Distortion Products versus Two-Tone Spacing — AFT21S230S

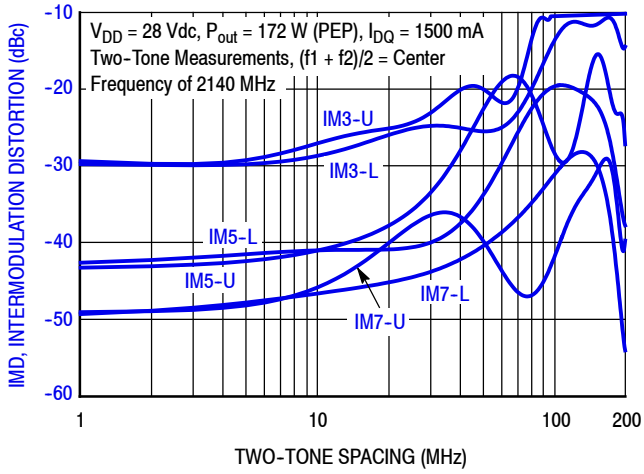


Figure 6b. Intermodulation Distortion Products versus Two-Tone Spacing — AFT21S232S

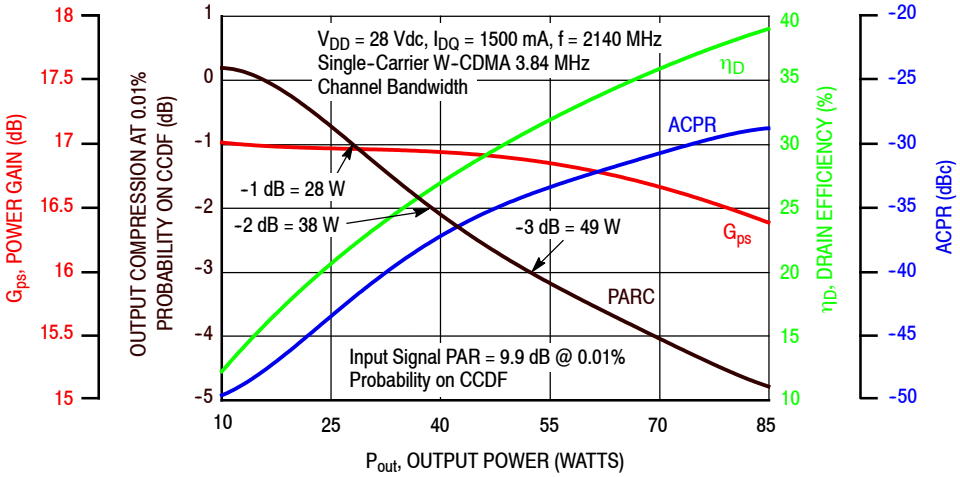


Figure 7. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

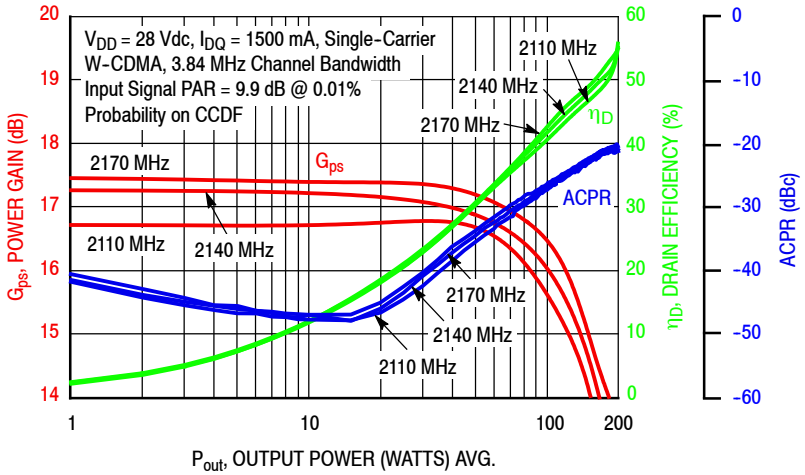


Figure 8. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

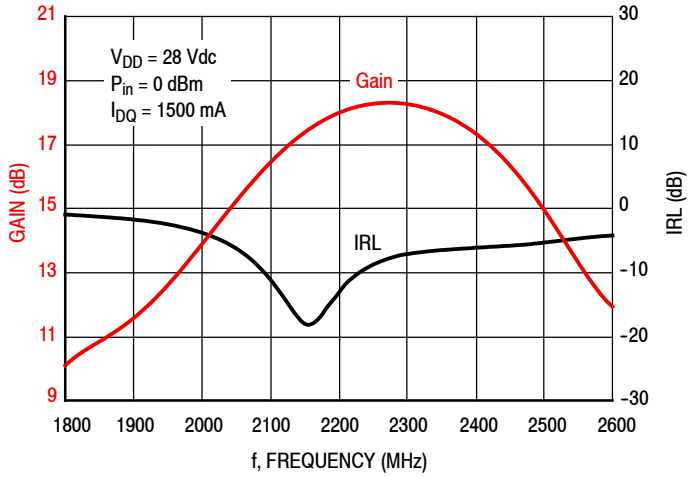


Figure 9. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQ} = 1500 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Max Linear Gain (dB)	Max Output Power							
					P1dB				P3dB			
					(dBm)	(W)	η_D (%)	AM/PM (°)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	1.20 - j6.00	1.20 + j5.90	1.50 - j3.90	17.7	54.3	269	55.4	11	55.2	331	57.0	16
2140	1.70 - j6.40	1.50 + j6.30	1.60 - j4.00	17.7	54.3	269	55.1	10	55.2	331	56.0	15
2170	1.70 - j6.80	1.75 + j6.70	1.50 - j4.00	17.8	54.3	269	54.7	11	55.2	331	56.0	16

(1) Load impedance for optimum P1dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

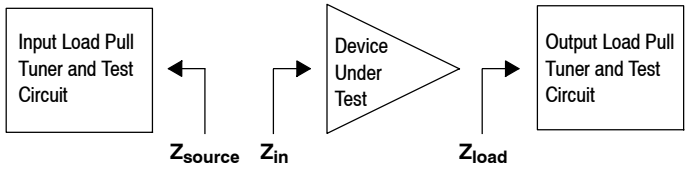


Figure 10. Load Pull Performance — Maximum P1dB Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1500 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Max Linear Gain (dB)	Max Drain Efficiency							
					P1dB				P3dB			
					(dBm)	(W)	η_D (%)	AM/PM (°)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	1.20 - j6.00	1.20 + j5.93	2.10 - j2.41	20.0	52.7	186	64.9	16	54.3	269	66.2	20
2140	1.70 - j6.40	1.40 + j6.30	1.80 - j2.60	19.8	52.8	191	64.2	16	53.4	219	65.4	24
2170	1.70 - j6.80	1.80 + j6.80	1.70 - j2.60	20.0	52.8	191	64.2	17	54.2	263	65.5	22

(1) Load impedance for optimum P1dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

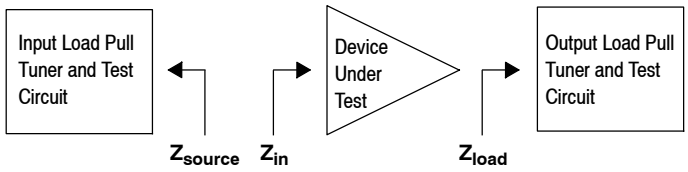


Figure 11. Load Pull Performance — Maximum Drain Efficiency Tuning

P1dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

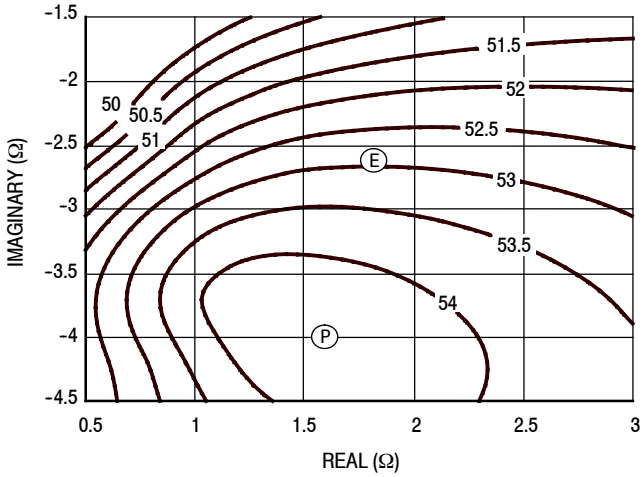


Figure 12. P1dB Load Pull Output Power Contours (dBm)

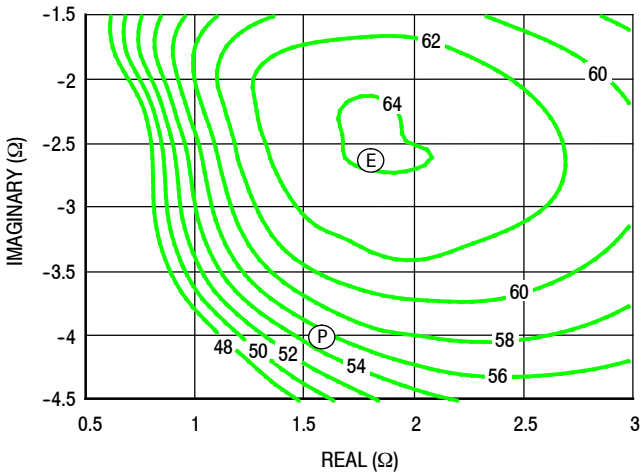


Figure 13. P1dB Load Pull Efficiency Contours (%)

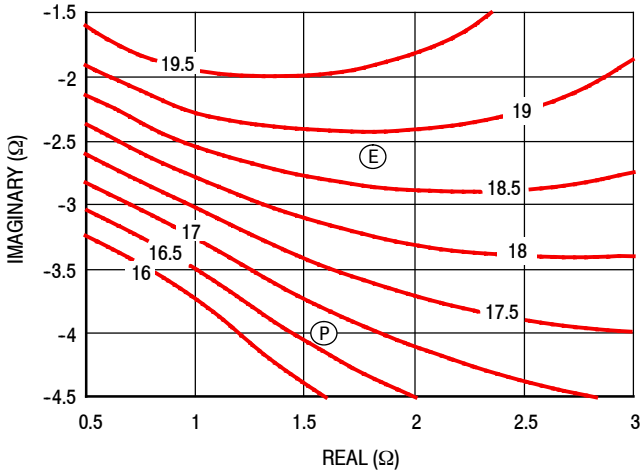


Figure 14. P1dB Load Pull Gain Contours (dB)

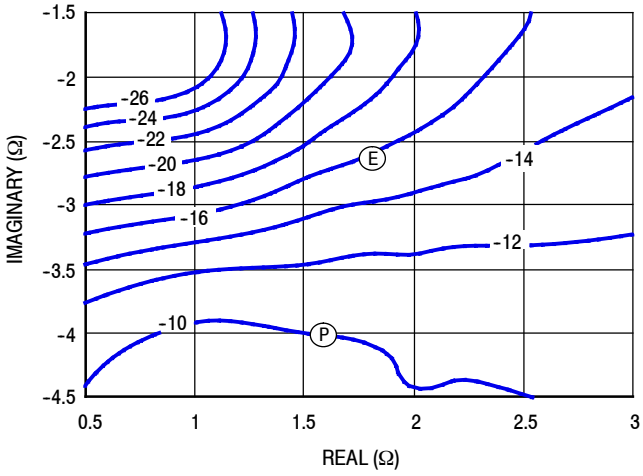


Figure 15. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

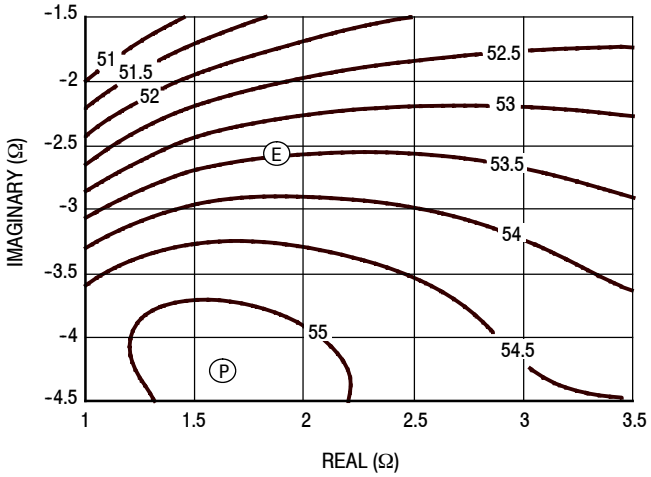


Figure 16. P3dB Load Pull Output Power Contours (dBm)

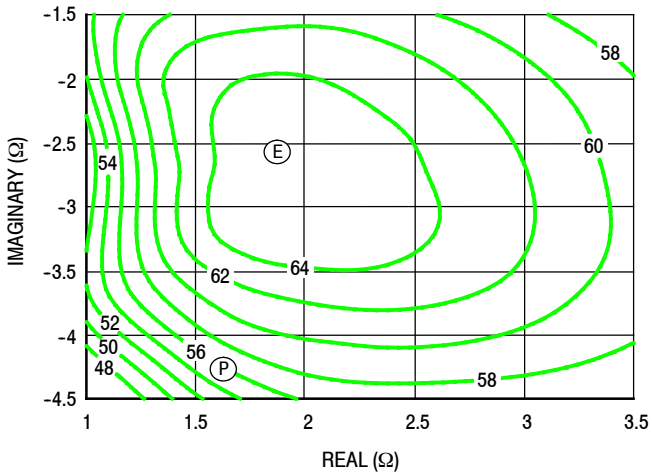


Figure 17. P3dB Load Pull Efficiency Contours (%)

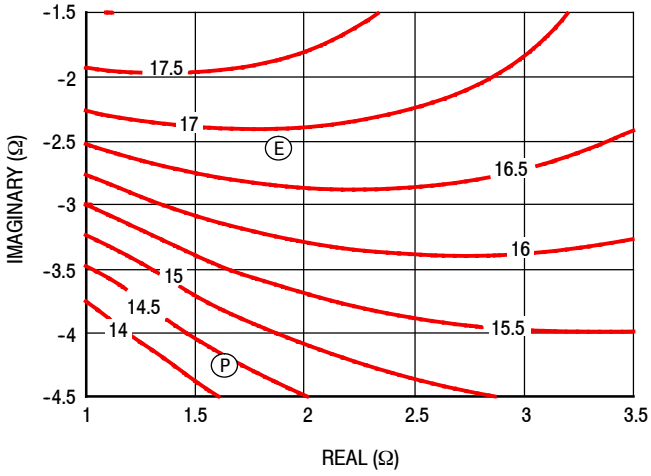


Figure 18. P3dB Load Pull Gain Contours (dB)

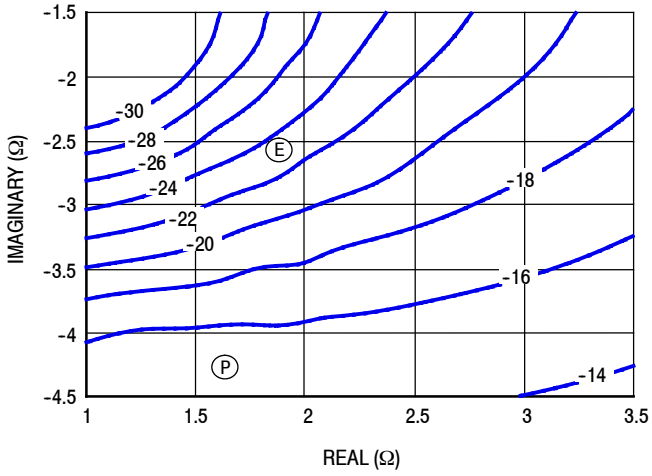


Figure 19. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

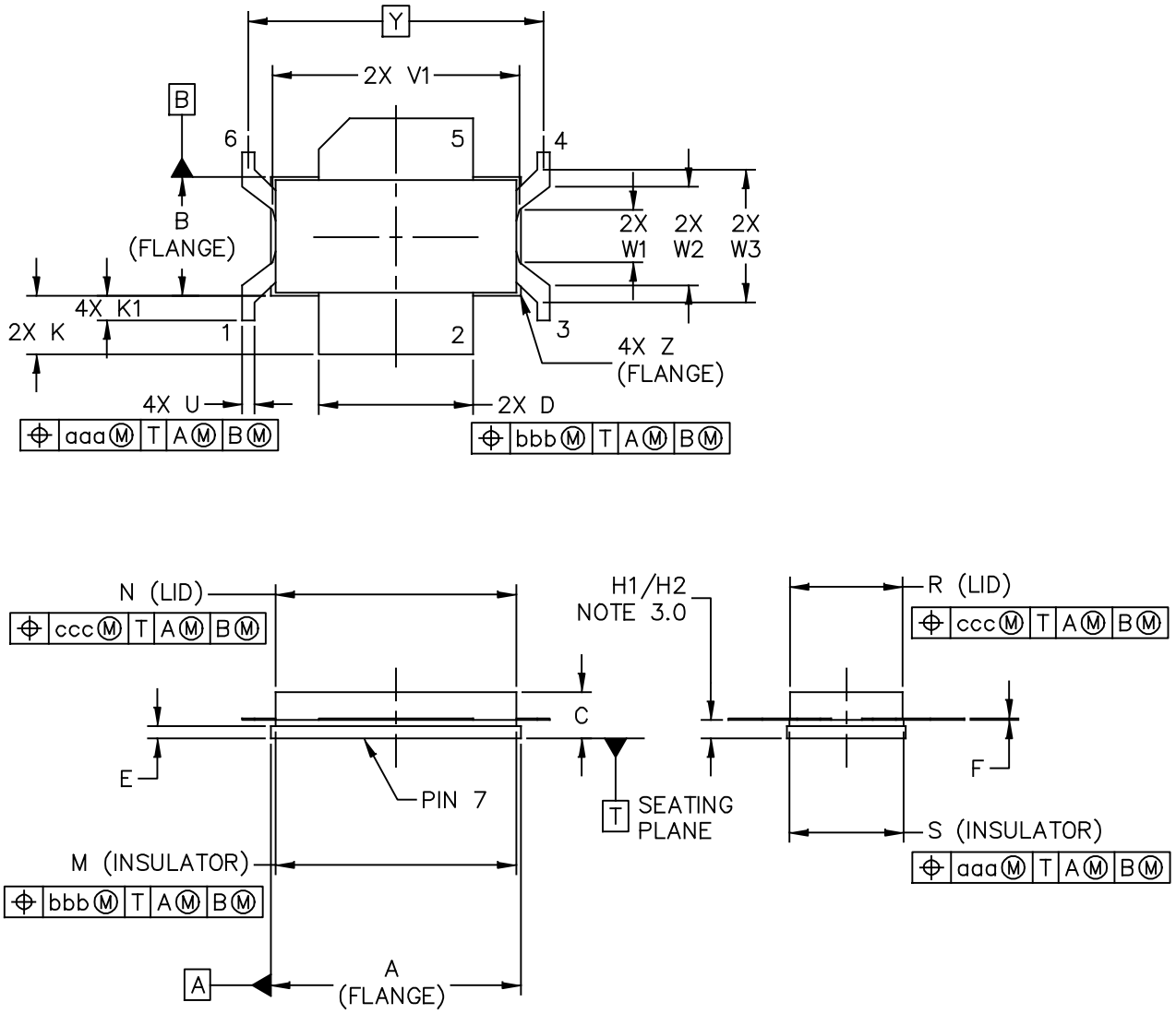
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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TITLE: NI-780S-6	DOCUMENT NO: 98ASA00443D	REV: A
	CASE NUMBER: 2268-02	24 MAY 2012
	STANDARD: NON-JEDEC	

NOTES:

1.0 CONTROLLING DIMENSION: INCH.

2.0 INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3.0 DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 2 & 5. H2 APPLIES TO PINS 1, 3, 4 & 6.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
B	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
C	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
D	.495	.505	12.57	12.83	V1	.795	.805	20.19	20.45
E	.035	.045	0.89	1.14	W1	.165	.175	4.19	4.45
F	.004	.007	0.10	0.18	W2	.315	.325	8.00	8.26
H1	.057	.067	1.45	1.70	W3	.425	.435	10.80	11.05
H2	.054	.070	1.37	1.78	Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R.00	R1.02
K1	.070	.090	1.78	2.29	aaa	–	.005	–	0.127
M	.774	.786	19.66	19.96	bbb	–	.010	–	0.254
N	.772	.788	19.61	20.02	ccc	–	.015	–	0.381

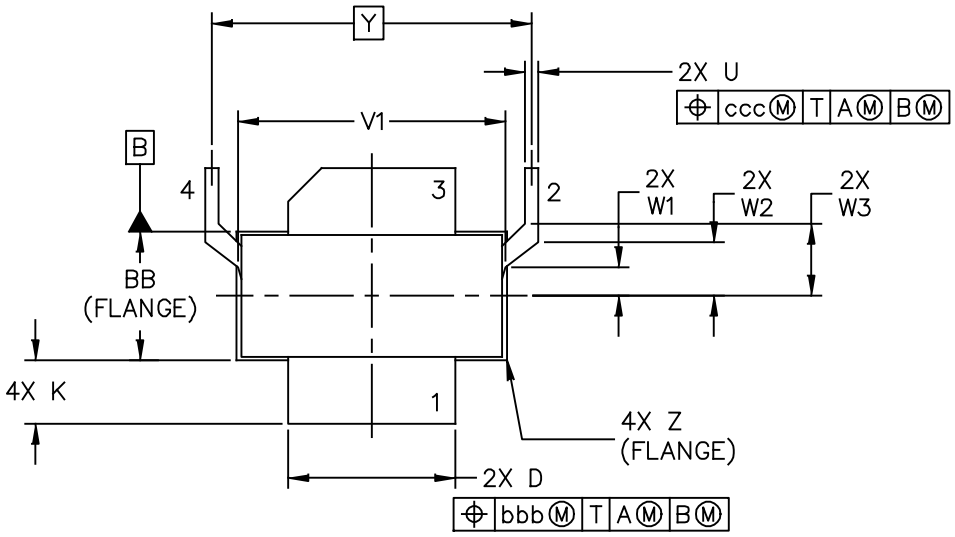
MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

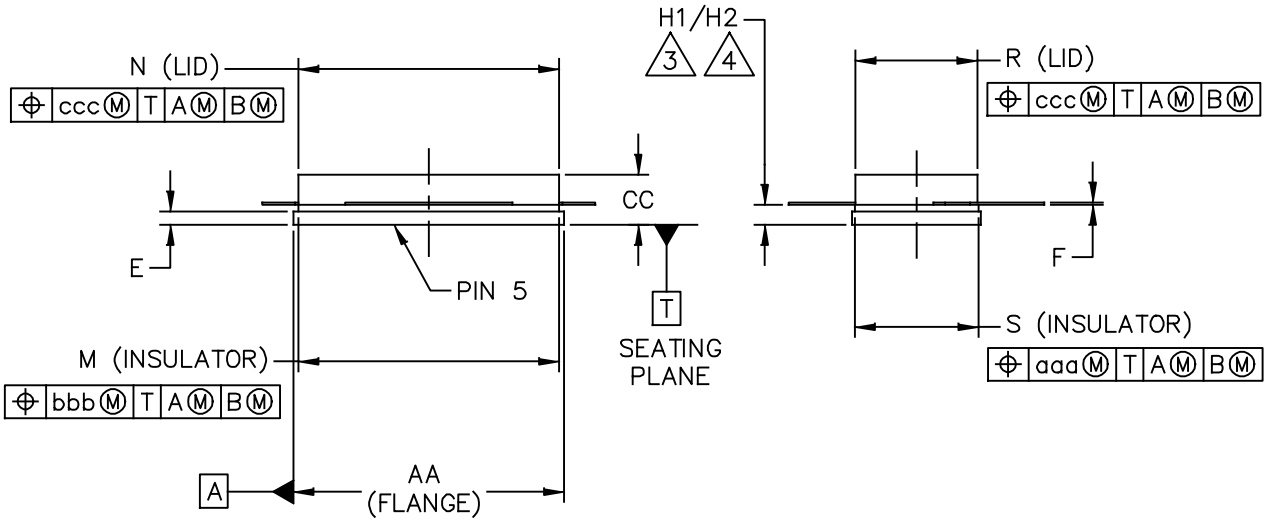
TITLE: NI–780S–6

DOCUMENT NO: 98ASA00443D | REV: A

CASE NUMBER: 2268–02 | 24 MAY 2012

STANDARD: NON–JEDEC





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TITLE: NI-780-2S2L	DOCUMENT NO: 98ASA00517D	REV: A
	STANDARD: NON-JEDEC	
	08 MAR 2013	

NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1 & 3. H2 APPLIES TO PINS 2 & 4.
4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
D	.495	.505	12.57	12.83	V1	.795	.805	20.19	20.45
E	.035	.045	0.89	1.14	W1	.080	.090	2.03	2.29
F	.004	.007	0.10	0.18	W2	.155	.165	3.94	4.19
H1	.057	.067	1.45	1.70	W3	.210	.220	5.33	5.59
H2	.054	.070	1.37	1.78	Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R0.00	R1.02
M	.774	.786	19.66	19.96	aaa	–	.005	–	0.13
N	.772	.788	19.61	20.02	bbb	–	.010	–	0.25
					ccc	–	.015	–	0.38

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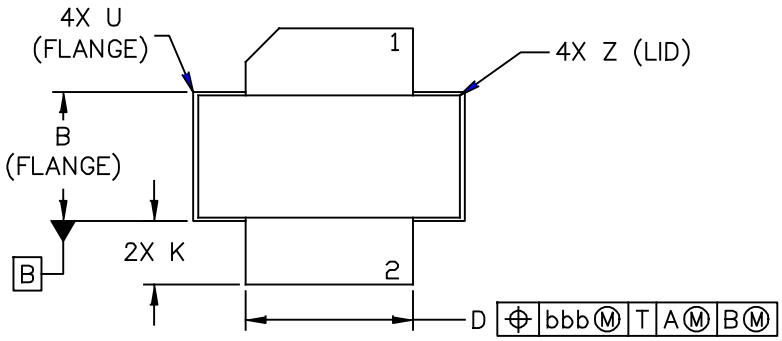
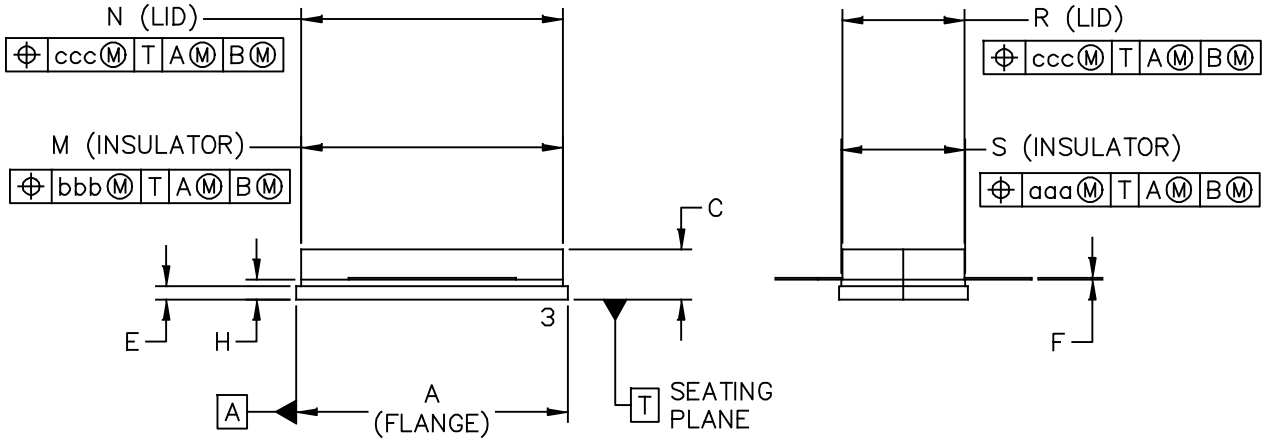
TITLE: NI–780–2S2L

DOCUMENT NO: 98ASA00517D REV: A

STANDARD: NON–JEDEC

08 MAR 2013





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	CASE NUMBER: 465A-06	31 MAR 2005
	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.805	.815	20.45	20.7	U	—	.040	—	1.02
B	.380	.390	9.65	9.91	Z	—	.030	—	0.76
C	.125	.170	3.18	4.32	aaa	—	.005	—	0.127
D	.495	.505	12.57	12.83	bbb	—	.010	—	0.254
E	.035	.045	0.89	1.14	ccc	—	.015	—	0.381
F	.003	.006	0.08	0.15	—	—	—	—	—
H	.057	.067	1.45	1.7	—	—	—	—	—
K	.170	.210	4.32	5.33	—	—	—	—	—
M	.774	.786	19.61	20.02	—	—	—	—	—
N	.772	.788	19.61	20.02	—	—	—	—	—
R	.365	.375	9.27	9.53	—	—	—	—	—
S	.365	.375	9.27	9.52	—	—	—	—	—

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

R5 TAPE AND REEL OPTION

NI-780S-2L4S: R5 Suffix = 50 Units, 44 mm Tape Width, 13-inch Reel.
NI-780S-2L: R5 Suffix = 50 Units, 56 mm Tape Width, 13-inch Reel.

The R5 tape and reel option for AFT21S230S and AFT21S232S parts will be available for 2 years after release of AFT21S230S and AFT21S232S. Freescale Semiconductor, Inc. reserves the right to limit the quantities that will be delivered in the R5 tape and reel option. At the end of the 2 year period customers who have purchased this device in the R5 tape and reel option will be offered AFT21S230S and AFT21S232S in the R3 tape and reel option.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2012	• Initial Release of Data Sheet
1	Nov. 2012	• Corrected Tape and Reel tape width from 32 mm to 44 mm, pp. 1, 17
2	Mar. 2013	• Table 1. Maximum Ratings, CW Operation for drain lead: changed CW Operation @ T_C = 25°C from 163 W to 161 W and changed derate factor from 0.79 W/°C to 0.75 W/°C to reflect recent thermal measurement test results of the AFT21S230S and AFT21S232S parts, p. 2 • Table 1. Maximum Ratings: added CW Operation rating and derate factor if the AFT21S230S part is biased through pin 4 and pin 6, p. 2 • Table 4. Load Mismatch: added footnote 2, indicating CW output power and CW rated power exceed recommended operating conditions, p. 3
3	Mar. 2014	• Added part number AFT21S230-12SR3, p. 1 • Added NI–780S–2L2L package isometric, p. 1, and Mechanical Outline, pp. 12-13 • Added Fig. 2, Pin Connections drawing for AFT21S230-12SR3 and VBW lead DC feed connecvtions footnote for AFT21S230SR3 and AFT21S230-12SR3, p. 1 • Maximum Ratings table, CW operation: added AFT21S230-12S part to VBW lead DC feed condition information, pp. 2-3 • Table 5, Test Circuit Component Designations and Values: updated PCB description to reflect most current board specifications from Rogers, p. 4

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