21143 PCI/CardBus 10/100Mb/s Ethernet LAN Controller

Brief Datasheet

Product Features

21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller (21143) is a single-chip device that supports direct memory access (DMA) and has direct interfaces to both the CardBus and the PCI local bus. The 21143 is optimized for low-power PCI/CardBus based systems.

Power-Management and Power-Savings Features

- Supports all network device OnNow* requirements for PC 97 and PC.
- Compliant with the ACPI specification and the *PCI Bus Power Management Interface Specification*, Revision 1.0.
- Implements low-power management with two power-saving modes (sleep and snooze).
- Supports Magic Packet technology and SecureON*, which is an additional security feature for Magic Packet.
- Supports dynamic clock control through clkrun over a PCI or CardBus* system.
- Implements low-power, 3.3-V CMOS technology.

Integration Features and Performance Advantages

- Contains onchip PCS and scrambler/descrambler for CAT5.
- Contains onchip integrated AUI port and a 10BASE-T transceiver.
- Provides an upgradable boot ROM interface up to 256KB.
- Supports PCI/CardBus read multiple, read line, and write and invalidate commands.
- Includes a powerful onchip DMA with programmable burst size, providing low CPU utilization.
- Supports an unlimited PCI/CardBus burst.
- Supports early interrupt and mitigation on transmit and receive.
- Contains a variety of flexible address filtering modes.

Device Features

- Provides MicroWire* interface for serial ROM (1K and 4K EEPROM).
- Supports CardBus status changed registers and CSTSCHG pin.
- Supports automatic loading of subvendor ID.
- Supports storage of CardBus card information structure (CIS) information (tuples) in the serial ROM or external flash ROM.
- Supports big or little endian byte ordering for buffers and descriptors.
- Supports PCI clock speed frequency from dc to 33 MHz; network operation with PCI clock from 20 MHz to 33 MHz.
- Supports full-duplex operation on both MII/SYM and 10BASE-T ports.
- Provides internal and external loopback capability on all network ports.
- Implements test-access port (JTAG compatible) with boundary-scan pins.

Automatic Detection/Sensing Features

- Enables automatic detection and correction of 10BASE-T receive polarity.
- Supports autodetection between AUI, 10BASE-T, and MII/SYM ports.
- Supports IEEE 802.3 Auto-Negotiation algorithm of full-duplex and half-duplex operation for 10 Mb/s and 100 Mb/s.

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Microarchitecture

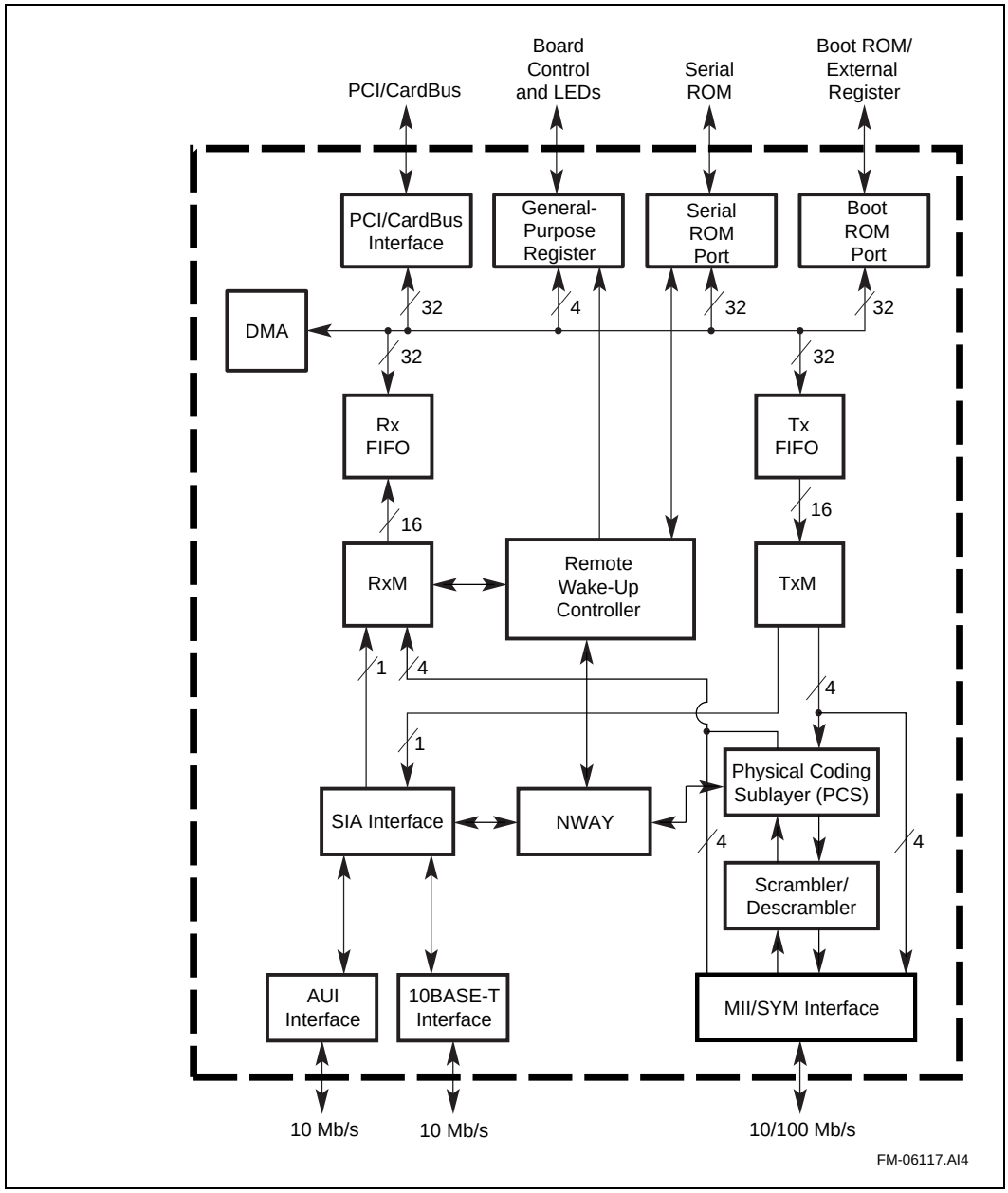
The 21143 direct interface to the PCI/CardBus local bus handles all PCI/CardBus control signals and executes PCI/CardBus DMA and I/O transactions. The 21143 DMA dual-receive and transmit controller handles all data transfers between external memory and onchip memory. The controller communicates with the host processor by using onchip command and status registers and a shared host memory area. Most of the required setup and initialization is done after power-up.

The 21143 microarchitecture features large transmit and receive FIFOs, a general-purpose register, a full MII signal interface, and a serial ROM port. The FIFOs eliminate the need for additional external memory, keeping the total solution cost low. The general-purpose register enables the software to use input or output functions and to control LED indicators for various network activities. The serial ROM port provides a direct interface to the MicroWire ROM for storage of Ethernet addresses and system parameters. The CIS can also be read from the serial ROM, eliminating the need for an external flash ROM.

The 21143 serial interface attachment (SIA) performs physical layer operations and implements the AUI and 10BASE-T functions, including the Manchester encode and decode operations. A direct connection to the 10BASE-T is made through the 10BASE-T port, and a direct connection to 10BASE2 and 10BASE5 is made through the AUI port.

The 21143 implements an MII-compliant interface to 10/100-Mb/s ENDEC for 100BASE-T4 and 100BASE-TX connections. In addition, the PCS and scrambler/descrambler function are integrated within the 21143, enabling operation with low-cost PHY devices, significantly reducing the cost of 100BASE-TX solutions. Figure 1 shows the functional units of the 21143 microarchitecture.

Figure 1. 21143 Block Diagram



Power Management

In support of industry initiatives, the 21143 is fully compliant with the *Network Device Class Power Management Specification, v.1.0* under the OnNow Architecture for Microsoft's *PC 97 Hardware Design Guide* and *PC 98 System Design Guide*. The 21143 is also fully compliant with the *Advanced Configuration and Power Interface* (ACPI) *Specification,* Revision 1.0 and the *PCI Bus Power Management Interface Specification,* Revision 1.0. It supports all five device power states (D0, D1, D2, $D3_{hot,}$ $D3_{cold}$) defined in the ACPI specification and the *PCI Bus Power Management Interface Specification,* Revision 1.0. The 21143 also supports all wake-up events defined in the *Network Device Class Power Management Specification, v.1.0* including pattern matching (with VLAN support), link change, and Magic Packet with SecureON.

For systems that do not support the standard power-management specifications, the 21143 provides a remote wake-up-LAN mechanism as an alternative for power management.

System Application Examples

The 21143 is an industry-leading, highly integrated solution for a variety of applications, such as:

- Cost-effective, high-performance PCI-based 10/100-Mb/s Ethernet network interface cards
- High-performance, power-managed CardBus based 10/100-Mb/s Ethernet PC card and motherboard applications
- PCI-based internetworking applications, such as a Fast Ethernet switch or a Fast Ethernet router port

Figure 2 shows a PCI adapter design using the 21143 that is capable of interfacing to both the 10-Mb/s and 10/100-Mb/s Ethernet networks.

Figure 3 shows CardBus based adapter designs with the MII/SYM circuitry located remotely from the CardBus module (left side), and the MII/SYM circuitry residing on the CardBus module (right side). Both of these CardBus designs benefit from storing the CIS within the serial ROM, reducing the component count and the number of connections.

Complete Solution

The 21143 evaluation board kits provide all the tools necessary for hardware engineers to design a PCI adapter or a CardBus module for a variety of products. Both of these kits include an evaluation board with 100BASE-T and 10BASE-T connections. They also include the software drivers, documentation, schematics, and Gerber files.

Figure 2. 10-Mb/s and 10/100-Mb/s Fast Ethernet PCI Adapter

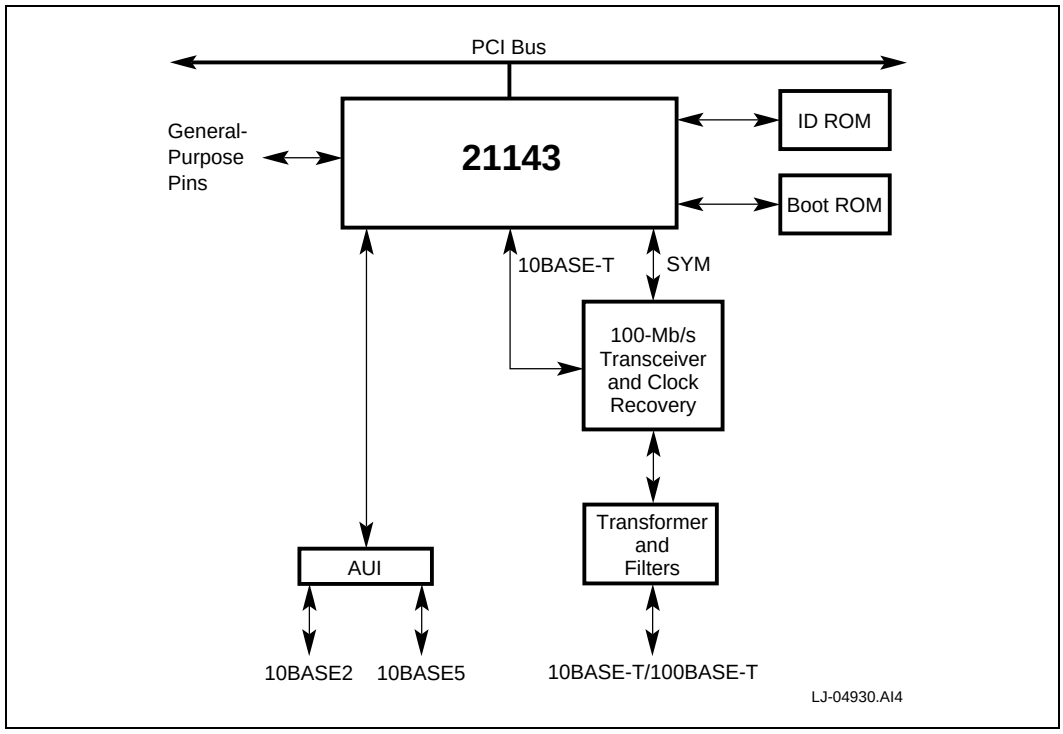
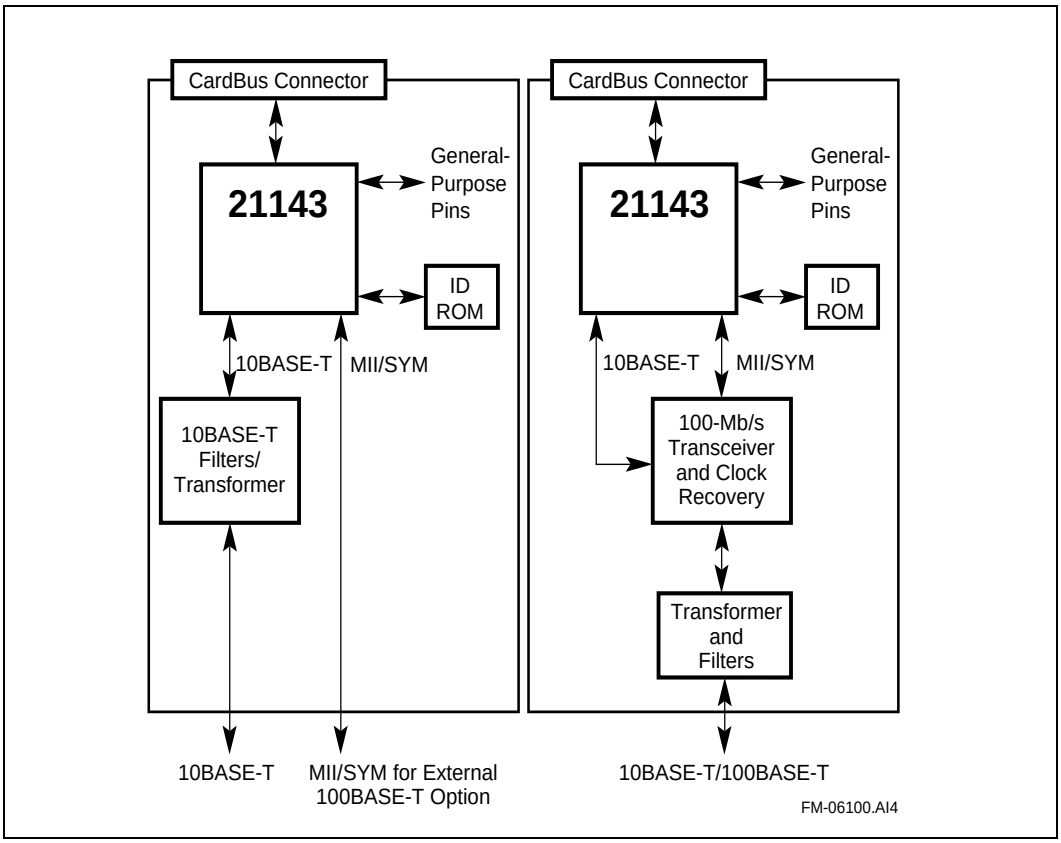


Figure 3. CardBus Applications



Characteristics	Specification
Power supply	Vdd 3.3 V Vdd_clamp=5 V or 3.3 V
Operating temperature	0°C to 70°C (32°F to 158°F)
Storage temperature range	–55°C to +125°C (–67°F to +257°F)
Power dissipation @Vdd = 3.3 V Frequency = 33-MHz PCI clock	75 mW to 560 mW[1]
Supply current after power-up	25 mA
Package	144-pin LQFP, 144-pin MQFP

1. Actual power dissipation depends upon the network activity and the power state of the device. Power values are based upon engineering estimates.

Support, Products, and Documentation

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