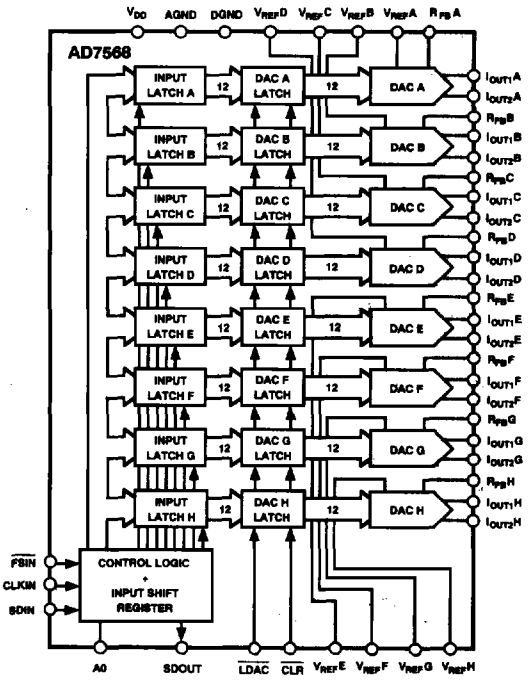
LC²MOS Octal 12-Bit DAC

AD7568

FEATURES
- Eight 12-Bit DACs in One Package
- 4-Quadrant Multiplication
- Separate References
- Single +5 V Supply
- Low Power: 1 mW
- Versatile Serial Interface
- Simultaneous Update Capability
- Reset Function
- 44-Pin PQFP and PLCC

APPLICATIONS
- Process Control
- Automatic Test Equipment
- General Purpose Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7568 contains eight 12-bit DACs in one monolithic device. The DACs are standard current output with separate V_{REF}, I_{OUT1}, I_{OUT2} and R_{FB} terminals.

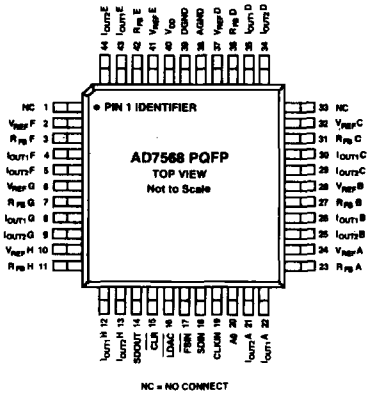
The AD7568 is a serial input device. Data is loaded using $\overline{FSIN}$, CLKIN and SDIN. One address pin, A0, sets up a device address, and this feature may be used to simplify device loading in a multi-DAC environment.

All DACs can be simultaneously updated using the asynchronous $\overline{LDAC}$ input and they can be cleared by asserting the asynchronous $\overline{CLR}$ input.

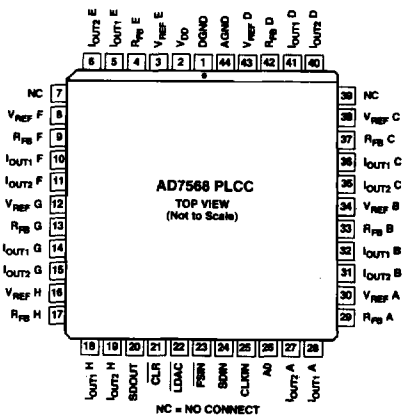
The AD7568 is housed in a space-saving 44-pin plastic quad flatpack and 44-lead PLCC.

PIN CONFIGURATIONS

Plastic Quad Flatpack



Plastic Leaded Chip Carrier



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7568—SPECIFICATIONS[1] (V_{DD} = +4.75 V to +5.25 V; I_{OUT1} = I_{OUT2} = 0 V; V_{REF} = +5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise stated)

Parameter	AD7568B[2]	Units	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	1 LSB = $V_{REF}/2^{12}$ = 1.22 mV when V_{REF} = 5 V
Relative Accuracy	±0.5	LSB max	
Differential Nonlinearity	±0.9	LSB max	All Grades Guaranteed Monotonic over Temperature
Gain Error			
+25°C	±4	LSBs max	
T_{MIN} to T_{MAX}	±5	LSBs max	
Gain Temperature Coefficient	2	ppm FSR/°C typ	
	5	ppm FSR/°C max	
Output Leakage Current			
I_{OUT1}			
@ +25°C	10	nA max	See Terminology Section
T_{MIN} to T_{MAX}	200	nA max	
REFERENCE INPUT			
Input Resistance	5	kΩ min	Typical Input Resistance = 7 kΩ
	9	kΩ max	
Ladder Resistance Mismatch	2	% max	Typically 0.6%
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±1	μA max	
C_{IN}, Input Capacitance	10	pF max	
POWER REQUIREMENTS			
V_{DD} Range	4.75/5.25	V min/V max	
Power Supply Sensitivity			
$\Delta Gain/\Delta V_{DD}$	−75	dB typ	
I_{DD}	300	μA max	V_{INH} = 4.0 V min, V_{INL} = 0.4 V max
	3.5	mA max	V_{INH} = 2.4 V min, V_{INL} = 0.8 V max

AC PERFORMANCE CHARACTERISTICS (These characteristics are included for Design Guidance and are not subject to test. DAC output op amp is AD843.)

Parameter	AD7568B[2]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	500	ns typ	To 0.01% of Full-Scale Range. DAC Latch Alternately Loaded with All 0s and All 1s.
Digital to Analog Glitch Impulse	40	nV–s typ	Measured with V_{REF} = 0 V. DAC Register Alternately Loaded with All 0s and All 1s.
Multiplying Feedthrough Error	−66	dB max	V_{REF} = 20 V pk–pk, 10 kHz Sine Wave. DAC Latch Loaded with All 0s.
Output Capacitance	60	pF max	All 1s Loaded to DAC.
	30	pF max	All 0s Loaded to DAC.
Channel-to-Channel Isolation	−76	dB typ	Feedthrough from Any One Reference to the Others with 20 V pk–pk, 10 kHz Sine Wave Applied.
Digital Crosstalk	40	nV–s typ	Effect of all 0s to all 1s Code Transition on Nonselected DACs.
Digital Feedthrough	40	nV–s typ	Feedthrough to Any DAC Output with $\overline{FSIN}$ High and Square Wave Applied to SDIN and SCLK.
Total Harmonic Distortion	−83	dB typ	V_{REF} = 6 V rms, 1 kHz Sine Wave.
Output Noise Spectral Density			
@ 1 kHz	20	$nV/\sqrt{Hz}$	All 1s Loaded to the DAC. V_{REF} = 0 V. Output Op Amp is AD OP-07.

NOTES
[1]Temperature range as follows: B Version: −40°C to +85°C.
[2]All specifications also apply for V_{REF} = +10 V, except relative accuracy which degrades to ±1 LSB.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{DD} = +5 V ± 5%; I_{OUT1} = I_{OUT2} = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Units	Description
t_1	100	100	ns min	CLKIN Cycle Time
t_2	40	40	ns min	CLKIN High Time
t_3	40	40	ns min	CLKIN Low Time
t_4	30	30	ns min	$\overline{FSIN}$ Setup Time
t_5	30	30	ns min	Data Setup Time
t_6	5	5	ns min	Data Hold Time
t_7	90	90	ns min	$\overline{FSIN}$ Hold Time
t_8[2]	70	70	ns max	SDOUT Valid After CLKIN Falling Edge
t_9	40	40	ns min	$\overline{LDAC}$, $\overline{CLR}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]t_8 is measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V.

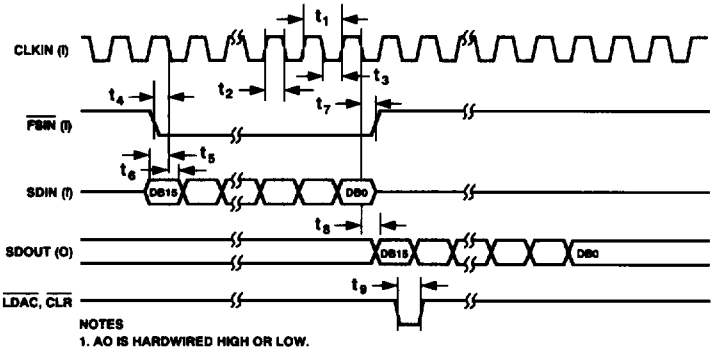


Figure 1. Timing Diagram

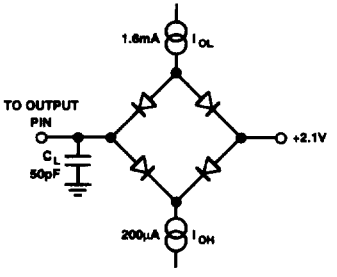


Figure 2. Load Circuit for Digital Output Timing Specifications

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSBs)	Package Option*
AD7568BS	−40°C to +85°C	±0.5	S-44
AD7568BP	−40°C to +85°C	±0.5	P-44A

*S = Plastic Quad Flatpack (PQFP), P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . −0.3 V to +6 V
I_{OUT1} to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
I_{OUT2} to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . −0.3 V to V_{DD} + 0.3 V
V_{RFB}, V_{REF} to DGND . . . . . ±15 V
Input Current to Any Pin Except Supplies[2] . . . . . ±10 mA
Operating Temperature Range
Commercial Plastic (B Versions) . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 250 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Table I. AD7568 Loading Sequence

DB15															DB0
DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	A0	DS2	DS1	DS0

Table II. DAC Selection

DS2	DS1	DS0	Function
0	0	0	DAC A Selected
0	0	1	DAC B Selected
0	1	0	DAC C Selected
0	1	1	DAC D Selected
1	0	0	DAC E Selected
1	0	1	DAC F Selected
1	1	0	DAC G Selected
1	1	1	DAC H Selected

TERMINOLOGY

Relative Accuracy
Relative Accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage or full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Gain Error
Gain Error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustable to zero with an external potentiometer.

Output Leakage Current
Output leakage current is current which flows in the DAC ladder switches when these are turned off. For the I_{OUT1} terminal, it can be measured by loading all 0s to the DAC and measuring the I_{OUT1} current. Minimum current will flow in the I_{OUT2} line when the DAC is loaded with all 1s. This is a combination of the switch leakage current and the ladder termination resistor current. The I_{OUT2} leakage current is typically equal to that in I_{OUT1}.

Output Capacitance
This is the capacitance from the I_{OUT1} pin to AGND.

Output Voltage Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For the AD7568, it is specified with the AD843 as the output op amp.

Digital to Analog Glitch Impulse
This is the amount of charge injected into the analog output when the inputs change state. It is normally specified as the area of the glitch in either pA-secs or nV-secs, depending upon whether the glitch is measured as a current or voltage signal. It is measured with the reference input connected to AGND and the digital inputs toggled between all 1s and all 0s.

AC Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC I_{OUT} terminal, when all 0s are loaded in the DAC.

Channel-to-Channel Isolation
Channel-to-channel isolation refers to the proportion of input signal from one DAC's reference input which appears at the output of any other DAC in the device and is expressed in dBs.

Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as the Digital Crosstalk and is specified in nV-secs.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up as noise on the I_{OUT} pin and subsequently on the op amp output. This noise is digital feedthrough.

AD7568—Typical Performance Curves

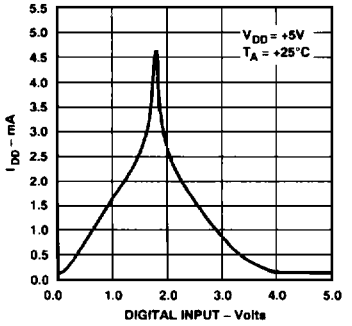


Figure 3. Supply Current vs. Logic Input Voltage

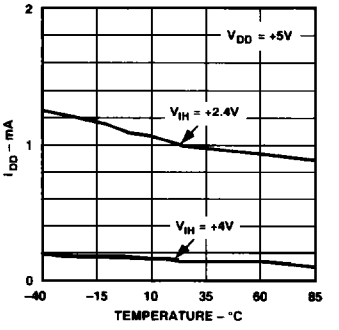


Figure 4. Supply Current vs. Temperature

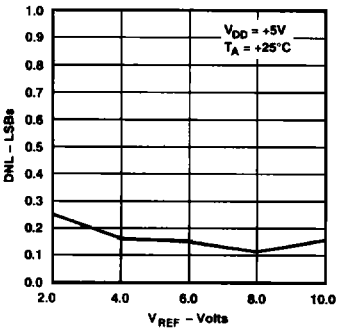


Figure 5. Differential Nonlinearity Error vs. V_{REF}

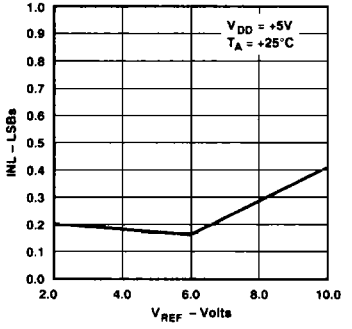


Figure 6. Integral Nonlinearity Error vs. V_{REF}

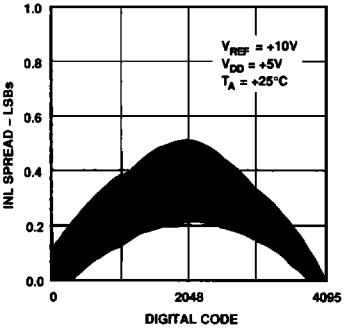


Figure 7. Typical DAC to DAC Linearity Matching

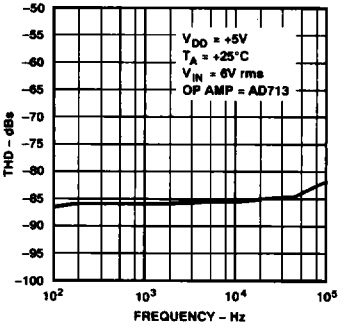


Figure 8. Total Harmonic Distortion vs. Frequency

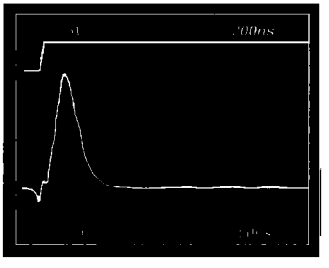


Figure 9. Digital-to-Analog Glitch Impulse

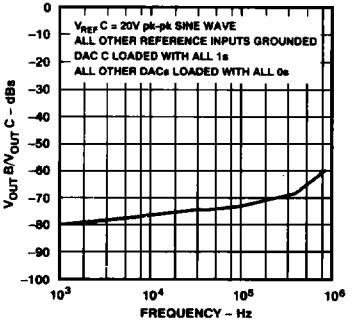


Figure 10. Channel-to-Channel Isolation (1 DAC to 1 DAC)

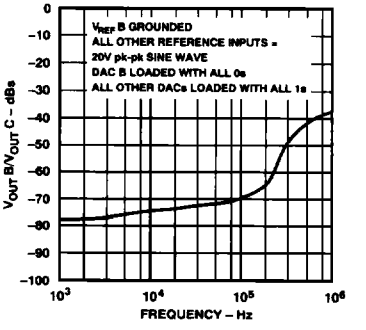


Figure 11. Channel-to-Channel Isolation (1 DAC to All Other DACs)