RoHS Compliant

Embedded Secure Digital Card

Datasheet

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Rev. 1.0

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FEATURES:

- **Fully compatible with SD card standard specification**
  - SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 2.00
  - SD Memory Card Specifications, Part 2, File System Specification, Version 2.00
  - SD Memory Card Specifications, Part 3, Security Specification, Version 2.00
- **NAND Flash Type**
  - SLC
- **Capacity**
  - Standard: 256MB, 512MB, 1GB, and 2GB
  - SDHC: 4GB
- **Performance**
  - Burst Read/Write: 25 MB/sec
  - Sustained Read/Write (MB/sec)

	Read	Write
Standard	11	8
ET*1	10	7

  - High-speed Sustained Read/Write (MB/sec)

	Read	Write
Standard	22	15
ET*1	16	10

- **SD-protocol compatible**
- **Support SPI mode**
- **Support SDHC Class 6**
- **Support auto standby and sleep mode**
- **Variable clock rate 0-50MHz**
- **Intelligent endurance design**
  - Built-in BCH-ECC supports correction up to 8 bits data error per 528 bytes data or 15 bits data error per 539 bytes data automatically
  - Implements dynamic wear-leveling algorithms to substantially increase longevity of flash media
  - Flash bad-block management
- **Temperature ranges**
  - Operating temperature

Standard	0°C ~ 70°C
ET*1	-40°C ~ 85°C

  - Storage temperature: -40°C ~ 100°C
- **Low power consumption**
- **Operation voltage: 2.7V ~ 3.6V**
- **Physical dimension: 24mm x 32mm x 2.1mm**
- **RoHS Compliant**

*1: Extended Temperature

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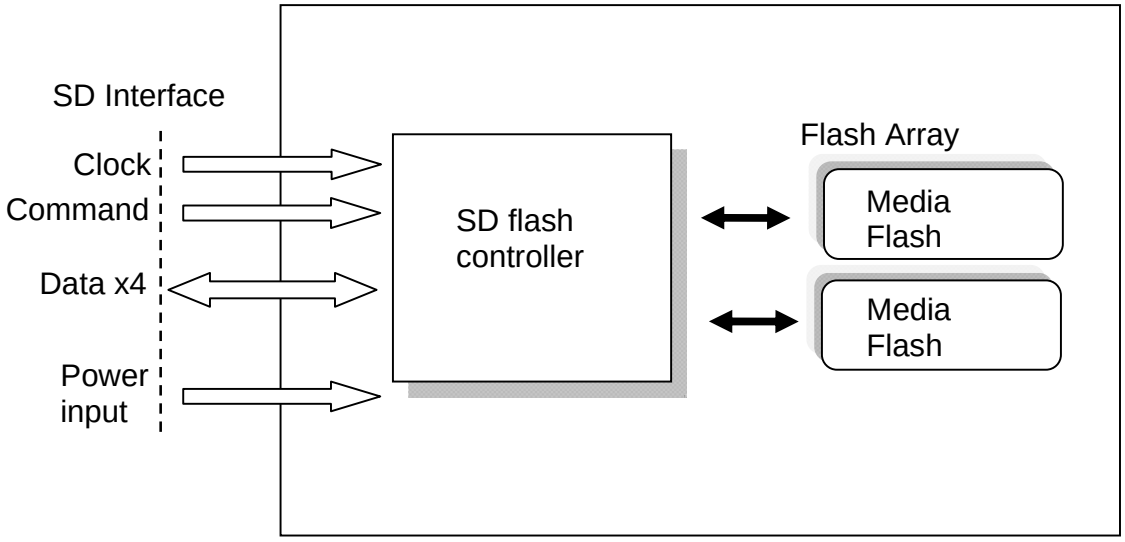
1. General Description

As embedded markets need for reliable and high-performance data storage in a small form factor becomes increasingly critical. The embedded SD card is designed specifically for demanding applications where extreme traceability, enhanced data integrity, and exceptionally fast read and write functionality are required.

Apacer's Embedded SD Card is offering higher endurance, reliability and performance, designed to meet the requirements of embedded applications.

1.1 Product Function Block

The embedded SD contains a flash controller and Flash Media with SD standard interface.



1.2 Functional description

The embedded SD device contains a high level, intelligent subsystem that provides many capabilities including:

- Host independence from details of erasing and programming flash memories.
- Powerful ECC algorithms
- Dynamic wear-leveling algorithms
- Power management for low power operation

1.2.1 Flash Management

The SD controller contains logic/physical flash block mapping and bad block management system. It will manage all flash block include user data space and spare block.

The embedded SD also contains a sophisticated defect and error management system. It does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the embedded SD replaces this bad bit with a spare bit within the sector header. If necessary, the embedded SD will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

1.2.2 Powerful ECC Algorithms

The powerful ECC algorithms will enhance flash block use rate and whole device life. The SD controller has an innovative algorithm to recover the data. Built-in BCH-ECC supports correction up to 8 bits data error per 528 bytes data or 15 bits data error per 539 bytes data automatically

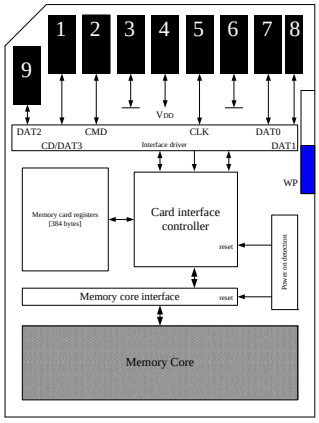
1.2.3 Power Management

A power saving feature of the embedded SD is automatic entrance and exit from sleep mode. Upon completion of an operation, the embedded SD will enter the sleep mode to conserve power if no further commands are received within X seconds, where X is programmable by software. The master does not have to take any action for this to occur. The embedded SD is in sleep mode except when the host is accessing it, thus conserving power.

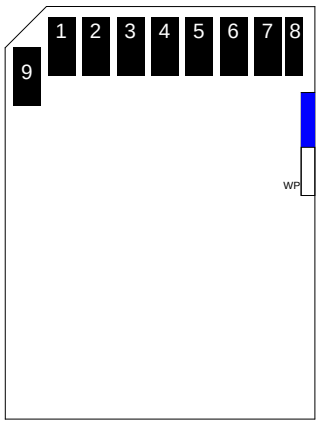
Any command issued by the master to the embedded SD will cause it to exit sleep mode and response to the master.

2. Electrical characteristics

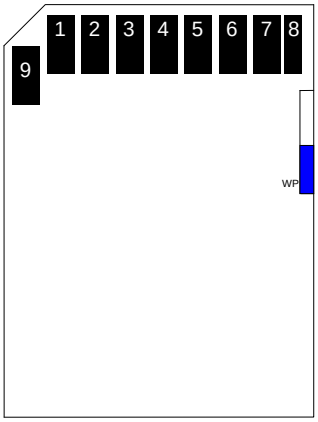
2.1 Card Architecture



Write Enabled



Write Protected



2.2 Pin Assignment

Pin	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	CD/DAT3	Card detect/Data line[Bit 3]	CS	Chip select
2	CMD	Command/Response	DI	Data in
3	VSS1	Supply voltage ground	VSS	Supply voltage ground
4	VDD	Supply voltage	VDD	Supply voltage
5	CLK	Clock	SCLK	Clock
6	VSS2	Supply voltage ground	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]	DO	Data out
8	DAT1	Data line[Bit 1]	Reserved	
9	DAT2	Data line[Bit 2]	Reserved	

2.3 Performance

The performance of Embedded SD

Operation		Transfer Rate (1MB = 1000Kbytes = 1000x1000 bytes)	
		Standard	ET[1]
Burst		25 MB/sec	
Read	Sustained(Notes)	Up to 11MB/sec	Up to 10MB/sec
Write	Sustained(Notes)	Up to 8 MB/sec	Up to 7 MB/sec
Read(SDHC)	High speed Sustained(Notes)	Up to 22 MB/sec	Up to 16 MB/sec
Write(SDHC)	High speed Sustained(Notes)	Up to 15 MB/sec	Up to 10 MB/sec
Block read access Time		Max. 80 ms	
Block write access Time		Max. 250 ms	
ACMD41 to ready after Power-up		Max. 750 ms	

Notes: Performance tested with HDBench v34b6 at 20MB transfer rate
*1: Extended Temperature

2.4 Capacity Specification

The Embedded SD product family is available as the table below. The following table shows the specific capacity. (Follow SDA rule to do format)

Standard

Capacity	Total (LBA) Sectors	Total Partition Sectors	User Data Sectors	User Data Bytes
256MB	496,640	496,539	496,384	254,148,608
512MB	967,680	967,439	967,168	495,190,016
1GB	1,967,616	1,967,363	1,966,848	1,007,026,176
2GB	3,935,232	3,934,979	3,934,464	2,014,445,568
4GB	7,934,976	7,926,784	7,918,528	4,054,286,336

ET[1]

Capacity	Total (LBA) Sectors	Total Partition Sectors	User Data Sectors	User Data Bytes
256MB	496,640	496,539	496,384	254,148,608
512MB	991,232	990,995	990,720	507,248,640
1GB	1,988,608	1,988,359	1,987,840	1,017,774,080
2GB	3,983,360	3,983,113	3,982,592	2,039,087,104
4GB	7,989,248	7,981,056	7,972,800	4,082,073,600

1: Extended Temperature

2.5 Recommended Operation Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Power Supply Voltage	2.7	3.3	3.6	V
Vss	Power Supply Voltage	0	0	0	V

2.6 Power consumption

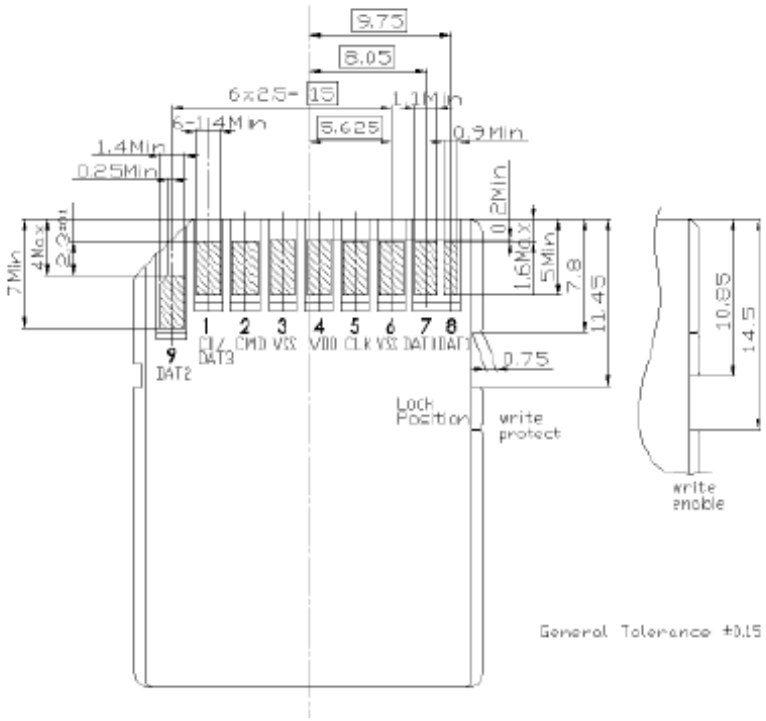
The Embedded SD requires operation voltage of 3.3V (DC).

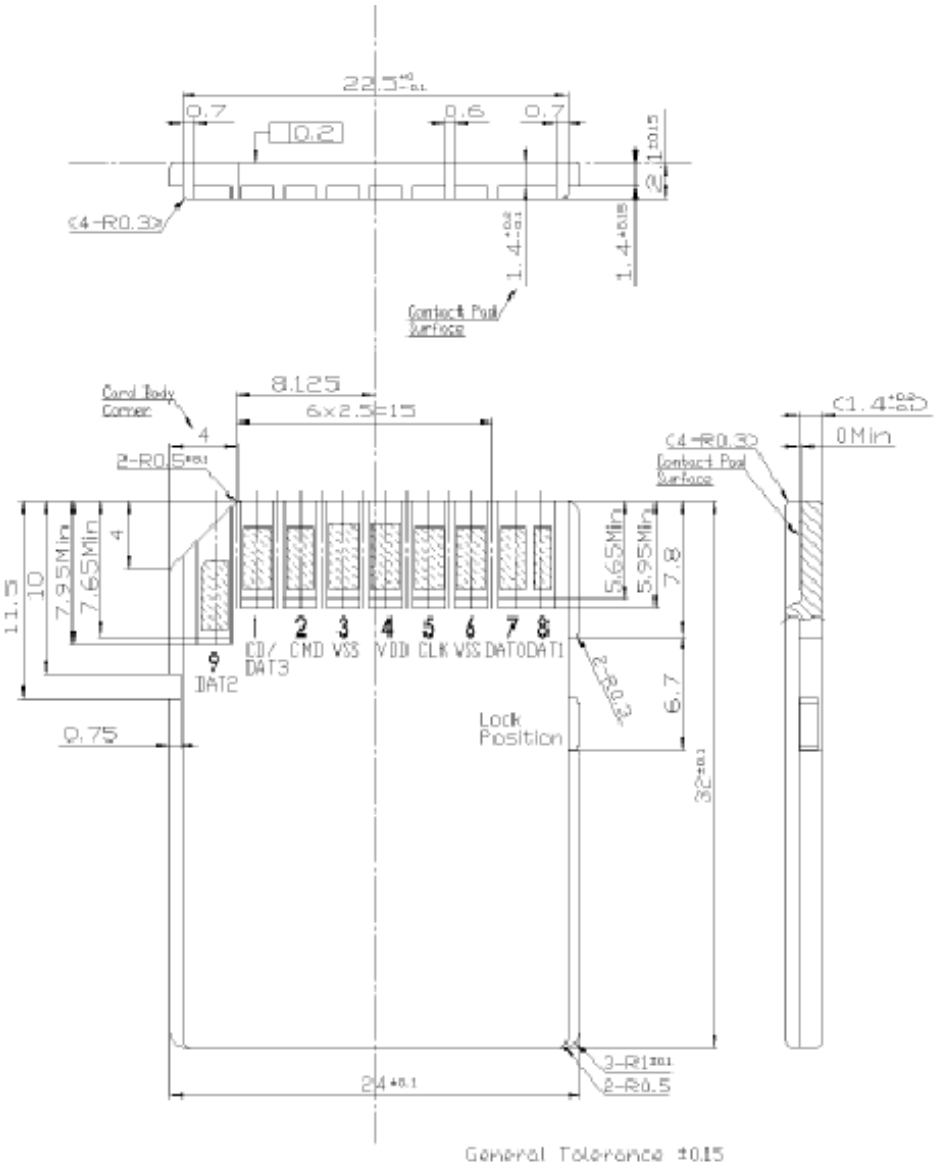
VCC 2.7V – 3.6V			
Mode	**Value**	**Unit**	**Average**
Sleep	160	uA	Max.
Read	23	mA	Typical
Write	41	mA	Typical

3. Physical Characteristics

3.1 Physical Dimension

Dimensions Card Package	24mmx32mm Min. 23.9mmx31.9mm Max.24.1mmx32.1mm
Thickness	2.1mm +/- 0.15mm
Surface	Plain (except contact area)
Edges	Smooth edges





3.2 System Reliability

Durability	10,000 mating cycles(Cycle time:500 cycles/hrs)
Data reliability	<1 non-recoverable error 10^{14} bits read
ECC ability	5 bytes

3.3 Environmental Specifications

Environmental Specification

Temperature	Operating	Standard: 0℃ to 70℃/ ET*1: -40℃ to 85℃
	Storage	-40℃ to 100℃
Humidity	Operating	25℃ - 95%RH non-condensing
	Non-operating	40℃ - 93%RH non-condensing
Salt Spray	Non-operating	5%wt NaCl Solution Temperature:35℃ 24hr
Bending	Non-operating	Apply Force 10N,Time ≧ 1min
Torque	Non-operating	torque = 0.15N.m or angle=+/-2.5 deg.(Max)
Drop	Non-operating	1.5m free fall
Minimum moving force of WP switch	Non-operating	Moving Force:40gf.(Ensures that the WP switch will not slide while it is inserted to the connector)
WP Switch cycles	Non-operating	Minimum 1,000 Cycles (cycle time:500 cycles/hrs) Slideforce:0.4N~5N

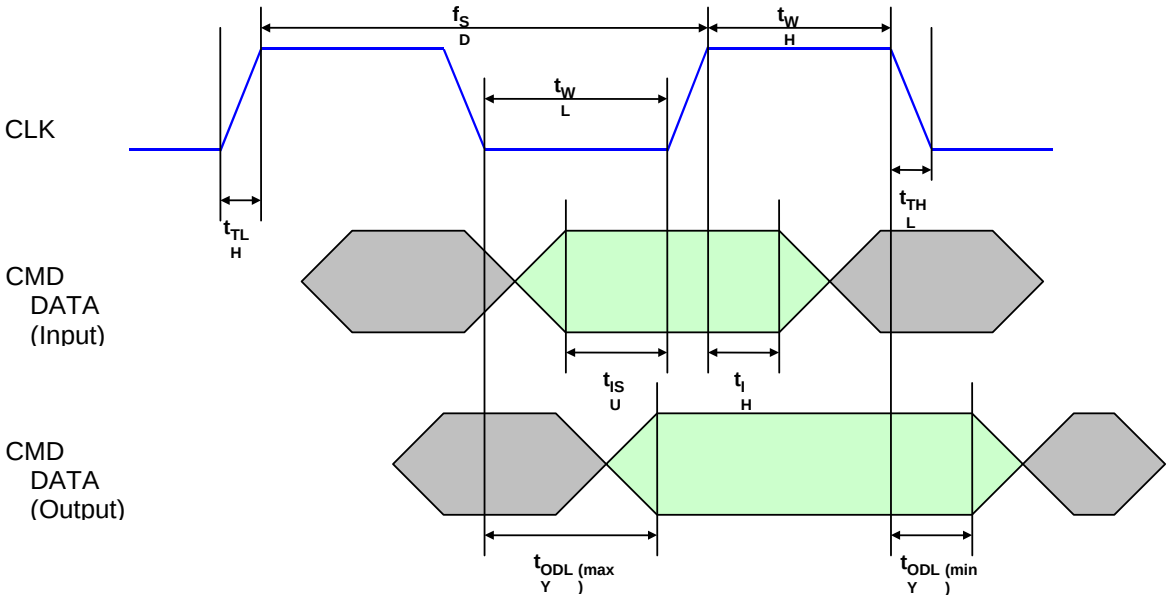
*1: Extended Temperature

4. AC Characteristics

4.1 Bus Timing – SD standard mode

SD Default Mode Bus Timing Parameter Value

SYMBOL	PARAMETER	MIN	MAX	UNIT	Note
f_{SD}	SD clock frequency	0	25	MHz	
t_{WL}	Clock low time	10	-	ns	
t_{WH}	Clock high time	10	-	ns	
t_{TLH}	Clock rise time	-	10	ns	
t_{THL}	Clock fall time	-	10	ns	
t_{ISU}	Input setup time	5	-	ns	
t_{IH}	Input hold time	5	-	ns	
t_{ODLY}	Output delay time	0	14	ns	

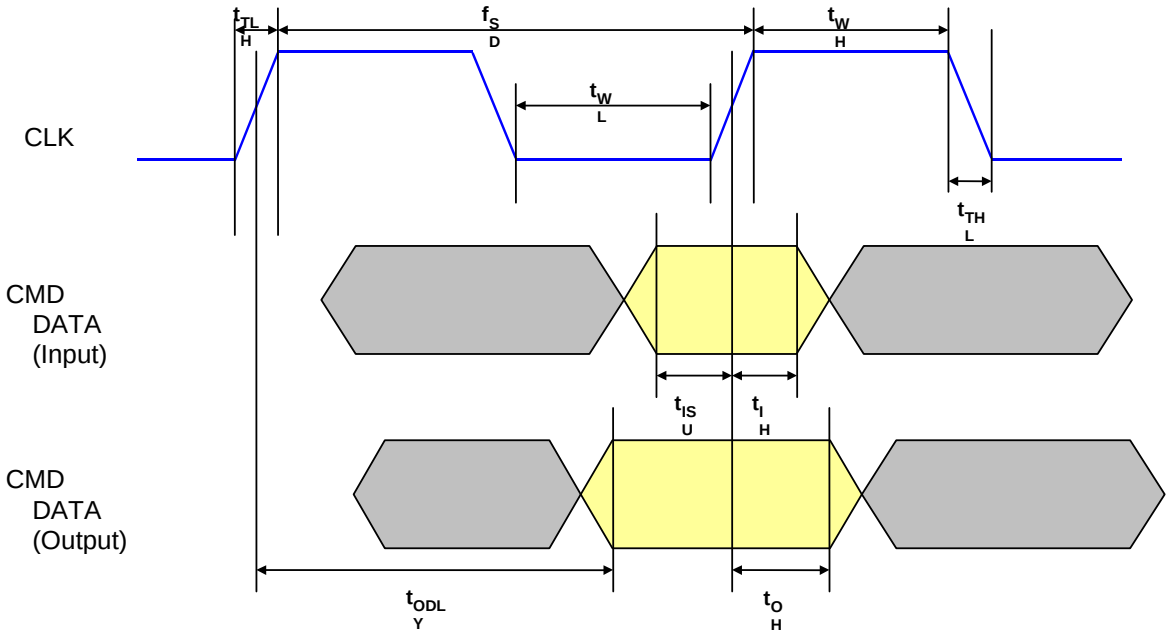


Timing Diagram of SD Default Mode Bus Timing

4.2 Bus Timing – SD High-speed mode

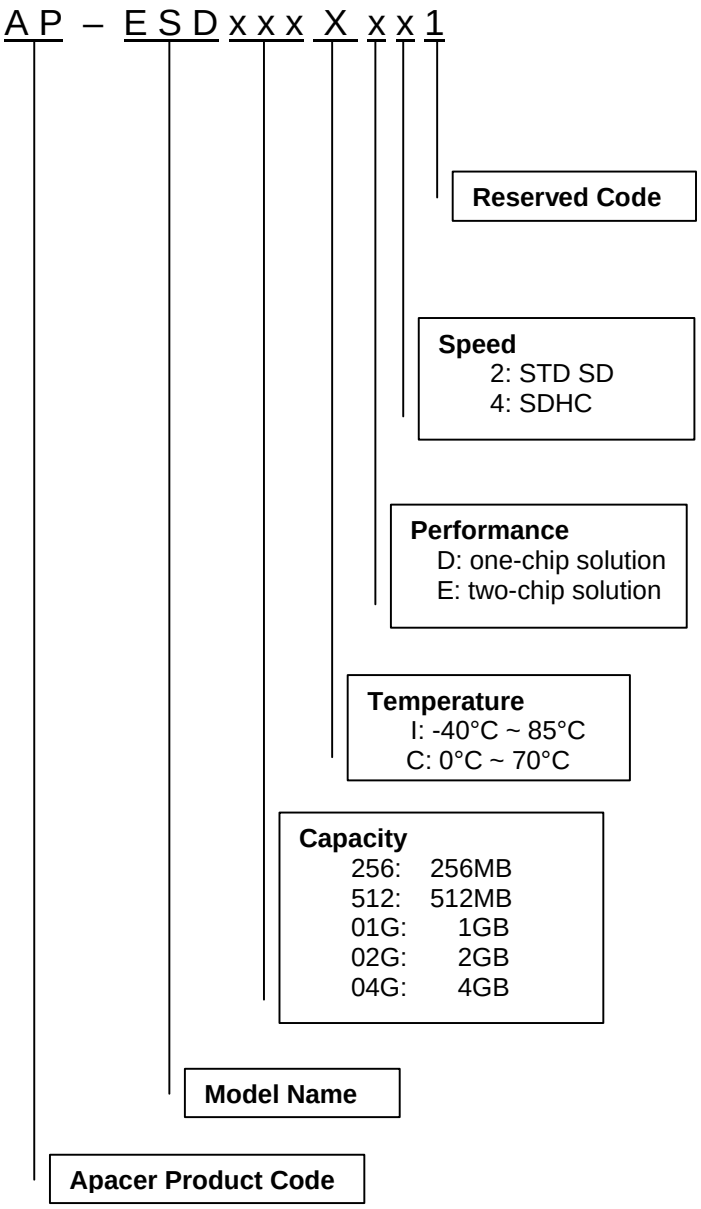
SD High-Speed Mode Bus Timing Parameter Value

SYMBOL	PARAMETER	MIN	MAX	UNIT	Note
f_{SD}	SD clock frequency	0	50	MHz	
t_{WL}	Clock low time	7	-	ns	
t_{WH}	Clock high time	7	-	ns	
t_{TLH}	Clock rise time	-	3	ns	
t_{THL}	Clock fall time	-	3	ns	
t_{ISU}	Input setup time	6	-	ns	
t_{IH}	Input hold time	2	-	ns	
t_{ODLY}	Output delay time	-	14	ns	
t_{OH}	Output hold time	2.5	-	ns	



Timing Diagram of SD High-Speed Mode Bus Timing

5. Product Ordering Information



5.1 Valid Combinations

Standard

Capacity	P/N
256MB	AP-ESD256CD21
512MB	AP-ESD512CD21
1GB	AP-ESD01GCD21
2GB	AP-ESD02GCD21
4GB	AP-ESD04GCE41

Extended Temperature

Capacity	P/N
256MB	AP-ESD256ID21
512MB	AP-ESD512ID21
1GB	AP-ESD01GID21
2GB	AP-ESD02GID21
4GB	AP-ESD04GIE41

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
0.1	Preliminary	November 14, 2008
1.0	Official release	January 19, 2009

Global Presence

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