

# 512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit (x8) Many-Time Programmable Flash SST37VF512 / SST37VF010 / SST37VF020 / SST37VF040



Data Sheet

## FEATURES:

- **Organized as 64K x8 / 128K x8 / 256K x8 / 512K x8**
- **2.7-3.6V Read Operation**
- **Superior Reliability**
  - Endurance: At least 1000 Cycles
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Current: 10 mA (typical)
  - Standby Current: 1  $\mu$ A (typical)
- **Fast Read Access Time**
  - 70 and 90 ns
- **Fast Byte-Program Operation**
  - Byte-Program Time: 10  $\mu$ s (typical)
  - Chip-Program Time:
    - 0.6 seconds (typical) for SST37VF512
    - 1.2 seconds (typical) for SST37VF010
    - 2.4 seconds (typical) for SST37VF020
    - 4.8 seconds (typical) for SST37VF040
- **Electrical Erase Using Programmer**
  - Does not require UV source
  - Chip-Erase Time: 100 ms (typical)
- **CMOS I/O Compatibility**
- **JEDEC Standard Byte-wide Flash EEPROM Pinouts**
- **Packages Available**
  - 32-Pin PDIP
  - 32-Pin PLCC
  - 32-Pin TSOP (8mm x 14mm)

## PRODUCT DESCRIPTION

The SST37VF512/010/020/040 devices are 64K x8 / 128K x8 / 256K x8 / 512K x8 CMOS, Many-Time Programmable (MTP), low cost flash, manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST37VF512/010/020/040 can be electrically erased and programmed at least 1000 times using an external programmer, e.g., to change the contents of devices in inventory. The SST37VF512/010/020/040 have to be erased prior to programming. These devices conform to JEDEC standard pinouts for byte-wide flash memories.

Featuring high performance Byte-Program, the SST37VF512/010/020/040 provide a typical Byte-Program time of 10  $\mu$ s. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with an endurance of at least 1000 cycles. Data retention is rated at greater than 100 years.

The SST37VF512/010/020/040 are suited for applications that require infrequent writes and low power nonvolatile storage. These devices will improve flexibility, efficiency, and performance while matching the low cost in nonvolatile applications that currently use UV-EPROMs, OTPs, and mask ROMs.

To meet surface mount and conventional through hole requirements, the SST37VF512/010/020/040 are offered in 32-pin PLCC, PDIP and TSOP packages. See Figures 1, 2 and 3 for pinouts.

## Device Operation

The SST37VF512/010/020/040 devices are nonvolatile memory solutions that can be used instead of standard flash devices if in-system programmability is not required. It is functionally (Read) and pin compatible with industry standard flash products. The device supports electrical Erase operation via an external programmer.

## Read

The Read operation of the SST37VF512/010/020/040 is controlled by CE# and OE#. Both CE# and OE# have to be low for the system to obtain data from the outputs. Once the address is stable, the address access time is equal to the delay from CE# to output ( $T_{CE}$ ). Data is available at the output after a delay of  $T_{OE}$  from the falling edge of OE#, assuming the CE# pin has been low and the addresses have been stable for at least  $T_{CE} - T_{OE}$ . When the CE# pin is high, the chip is deselected and a standby current of only 10  $\mu$ A (typical) is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is  $V_{IH}$ . Refer to Figure 4 for the timing diagram.

## Byte-Program Operation

The SST37VF512/010/020/040 are programmed by using an external programmer. The programming mode is activated by asserting 12V ( $\pm 5\%$ ) on OE# pin and  $V_{IL}$  on CE# pin. The device is programmed using a single pulse (WE# pin low) of 10  $\mu$ s per byte. Using the MTP programming algorithm, the Byte-Program process continues byte-by-byte until the entire chip has been programmed. Refer to Figure 10 for the flowchart and Figure 6 for the timing diagram.



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## Chip-Erase Operation

The only way to change a data from a “0” to “1” is by electrical erase that changes every bit in the device to “1”. The SST37VF512/010/020/040 use an electrical Chip-Erase operation. The entire chip can be erased in 100 ms (WE# pin low). In order to activate erase mode, the 12V ( $\pm 5\%$ ) is applied to OE# and A<sub>9</sub> pins while CE# is low. All other address and data pins are “don’t care”. The falling edge of WE# will start the Chip-Erase operation. Once the chip has been erased, all bytes must be verified for FF. Refer to Figure 9 for the flowchart and Figure 5 for the timing diagram.

## Product Identification Mode

The Product Identification mode identifies the devices as SST37VF512, SST37VF010, SST37VF020, and SST37VF040 and manufacturer as SST. This mode may be accessed by the hardware method. To activate this mode, the programming equipment must force V<sub>H</sub> (12V $\pm 5\%$ ) on address A<sub>9</sub>. Two identifier bytes may then be sequenced from the device outputs by toggling address line A<sub>0</sub>. For details, see Table 3 for hardware operation.

TABLE 1: PRODUCT IDENTIFICATION TABLE

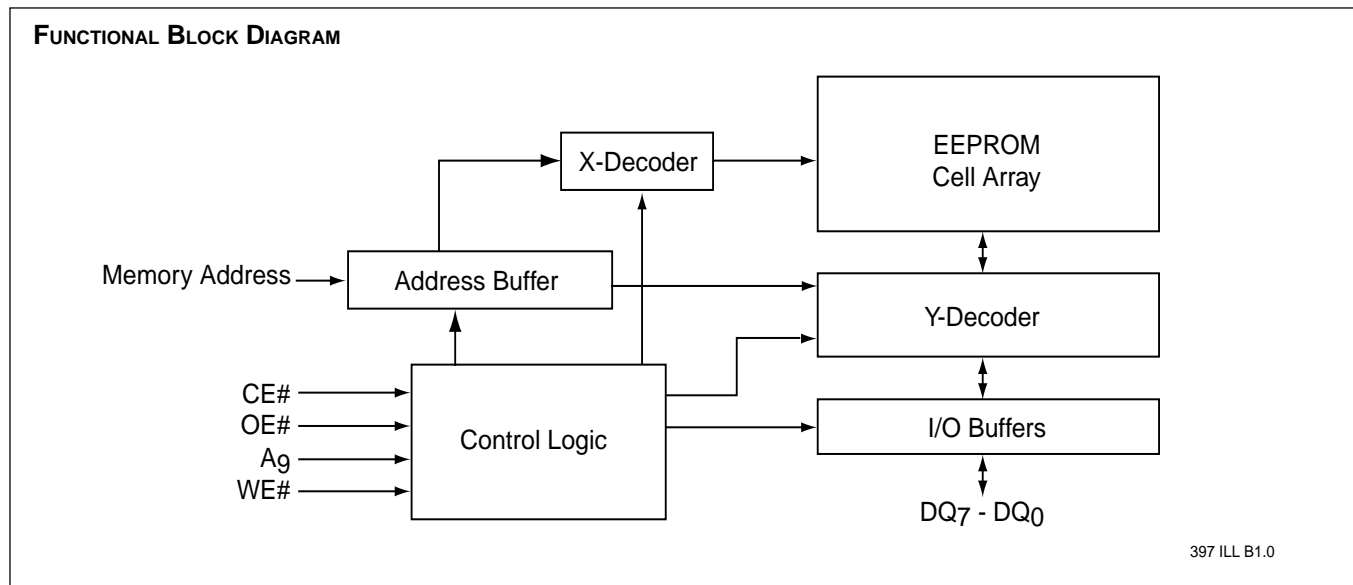
	Byte	Data
Manufacturer’s Code	0000 H	BF H
Device Code		
SST37VF512	0001 H	C4 H
SST37VF010	0001 H	C5 H
SST37VF020	0001 H	C6 H
SST37VF040	0001 H	C2 H

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## Design Considerations

The SST37VF512/010/020/040 should have a 0.1 $\mu$ F ceramic high frequency, low inductance capacitor connected between V<sub>DD</sub> and GND. This capacitor should be placed as close to the package terminals as possible.

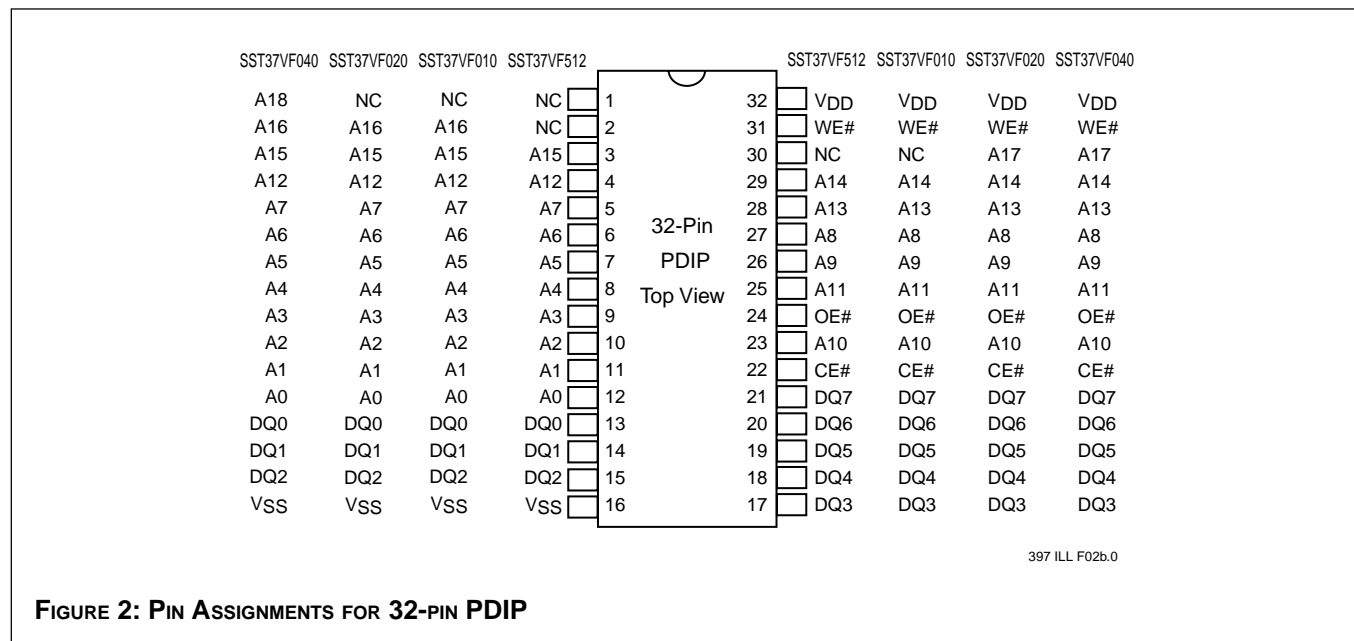
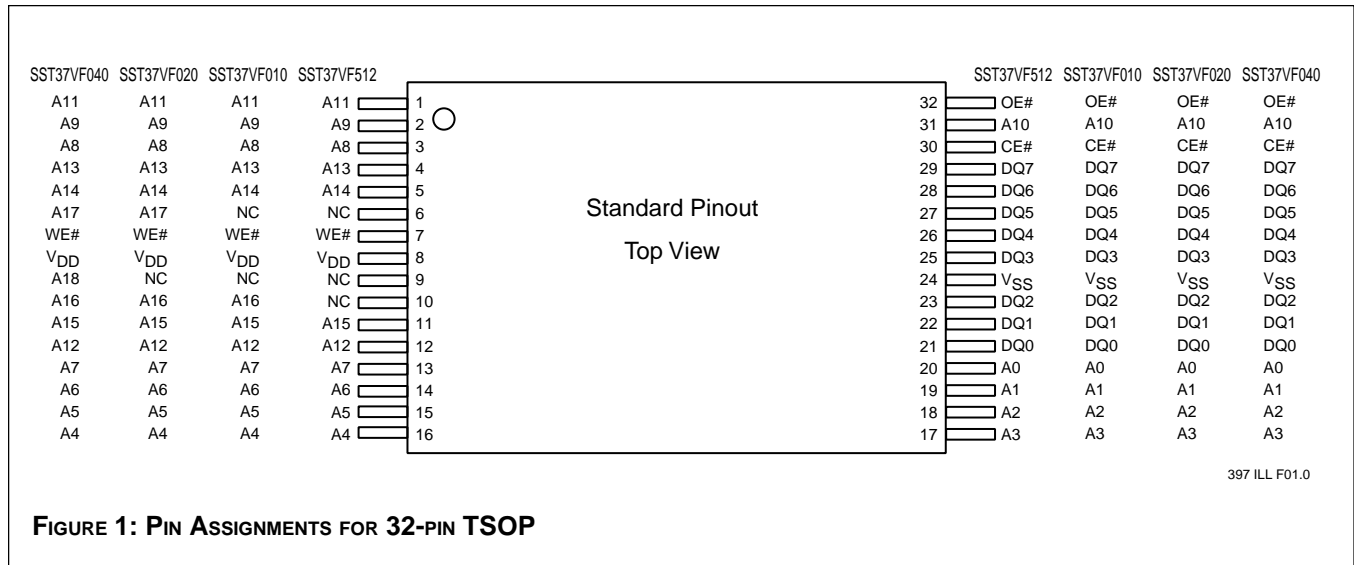
OE# and A<sub>9</sub> must remain stable at V<sub>H</sub> for the entire duration of an Erase operation. OE# must remain stable at V<sub>H</sub> for the entire duration of the Program operation.





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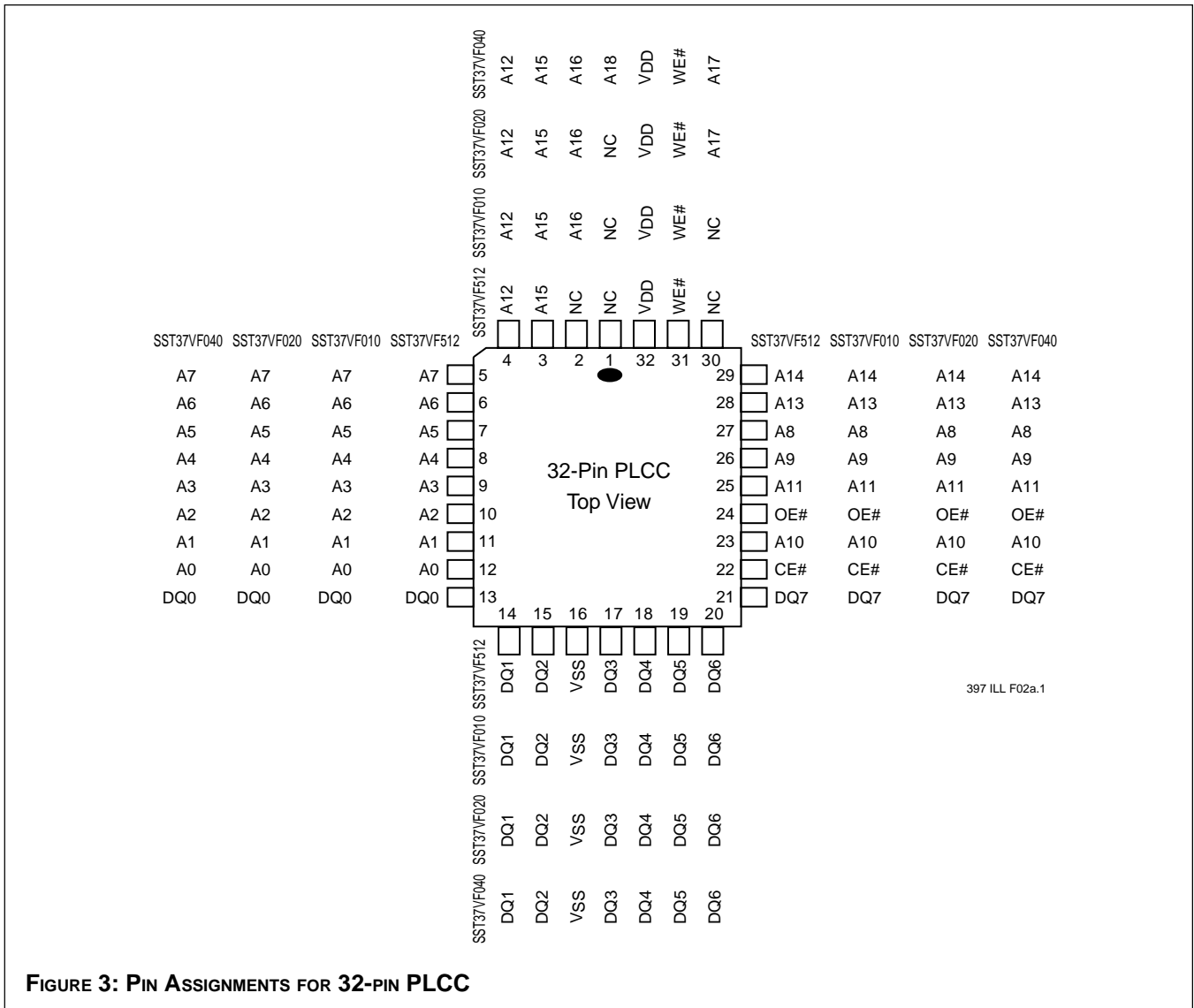
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**TABLE 2: PIN DESCRIPTION**

Symbol	Pin Name	Functions
AMS-A <sub>0</sub>	Address Inputs	To provide memory addresses
DQ <sub>7</sub> -DQ <sub>0</sub>	Data Input/Output	To output data during Read cycles and receive input data during Program cycle, the outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low
WE#	Write Enable	To program or erase (WE# = V <sub>IL</sub> pulse during Program or Erase)
OE#	Output Enable	To gate the data output buffers during Read operation when low
V <sub>DD</sub>	Power Supply	To provide 3-volt supply (2.7 to 3.6V)
V <sub>SS</sub>	Ground	
NC	No Connection	Unconnected pins

**Note:** AMS = Most significant address  
AMS = A<sub>15</sub> for SST37VF512, A<sub>16</sub> for SST37VF010, A<sub>17</sub> for SST37VF020 and A<sub>18</sub> for SST37VF040.

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**TABLE 3: OPERATION MODES SELECTION**

Mode	CE#	WE#	A <sub>9</sub>	OE#	DQ	Address
Read	V <sub>IL</sub>	V <sub>IH</sub>	A <sub>IN</sub>	V <sub>IL</sub>	D <sub>OUT</sub>	A <sub>IN</sub>
Output Disable	V <sub>IL</sub>	X	X	V <sub>IH</sub>	High Z	A <sub>IN</sub>
Standby	V <sub>IH</sub>	X	X	X	High Z	X
Chip-Erase	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>H</sub>	V <sub>H</sub>	High Z	X
Byte-Program	V <sub>IL</sub>	V <sub>IL</sub>	A <sub>IN</sub>	V <sub>H</sub>	D <sub>IN</sub>	A <sub>IN</sub>
Program/Erase	X	V <sub>IH</sub>	X	X	High Z	X
Inhibit	X	X	X	V <sub>IL</sub> or V <sub>IH</sub>	High Z/D <sub>OUT</sub>	X
Product Identification	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>H</sub>	V <sub>IL</sub>	Manufacturer Code (BF) Device Code (1)	A <sub>MS</sub> <sup>(2)</sup> -A <sub>1</sub> = V <sub>IL</sub> , A <sub>0</sub> = V <sub>IL</sub> A <sub>MS</sub> <sup>(2)</sup> -A <sub>1</sub> = V <sub>IL</sub> , A <sub>0</sub> = V <sub>IH</sub>

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- Note:** X = V<sub>IL</sub> or V<sub>IH</sub> (or V<sub>H</sub> in case of OE# and A<sub>9</sub>)  
V<sub>H</sub> = 12V±5%  
(1) Device code C4 for SST37VF512, C5 for SST37VF010, C6 for SST37VF020 and C2 for SST37VF040.  
(2) A<sub>MS</sub> = Most significant address  
A<sub>MS</sub> = A<sub>15</sub> for SST37VF512, A<sub>16</sub> for SST37VF010, A<sub>17</sub> for SST37VF020 and A<sub>18</sub> for SST37VF040.

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

- Temperature Under Bias ..... -55°C to +125°C
- Storage Temperature ..... -65°C to +150°C
- D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V<sub>DD</sub>+ 0.5V
- Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V<sub>DD</sub>+ 1.0V
- Voltage on A<sub>9</sub> and OE# Pin to Ground Potential ..... -0.5V to 13.2V
- Package Power Dissipation Capability (T<sub>A</sub> = 25°C) ..... 1.0W
- Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
- Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
- Output Short Circuit Current<sup>(1)</sup> ..... 50 mA

**Note:** <sup>(1)</sup> Outputs shorted for no more than one second. No more than one output shorted at a time.

**OPERATING RANGE**

Range	Ambient Temp	V <sub>DD</sub>
Commercial	0°C to +70°C	2.7 to 3.6V
Industrial	-40°C to +85°C	2.7 to 3.6V

**AC CONDITIONS OF TEST**

Input Rise/Fall Time ..... 5 ns
Output Load ..... C <sub>L</sub> = 100 pF
See Figures 7 and 8



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**TABLE 4: READ MODE DC OPERATING CHARACTERISTICS**  
**V<sub>DD</sub> = 2.7 to 3.6V, T<sub>A</sub> = 0°C to 70°C (Commercial)**

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I <sub>DD</sub>	V <sub>DD</sub> Read Current		12	mA	CE# = OE# = V <sub>IL</sub> , all I/Os open, Address Input = V <sub>IL</sub> /V <sub>IH</sub> , at f = 1/T <sub>RC</sub> Min, V <sub>DD</sub> = V <sub>DD</sub> Max
I <sub>SB</sub>	Standby V <sub>DD</sub> Current		15	μA	CE# = V <sub>IHC</sub> V <sub>DD</sub> = V <sub>DD</sub> Max
I <sub>LI</sub>	Input Leakage Current		1	μA	V <sub>IN</sub> = GND to V <sub>DD</sub> , V <sub>DD</sub> = V <sub>DD</sub> Max
I <sub>LO</sub>	Output Leakage Current		1	μA	V <sub>OUT</sub> = GND to V <sub>DD</sub> , V <sub>DD</sub> = V <sub>DD</sub> Max
V <sub>IL</sub>	Input Low Voltage		0.8	V	V <sub>DD</sub> = V <sub>DD</sub> Min
V <sub>IH</sub>	Input High Voltage	0.7 V <sub>DD</sub>		V	V <sub>DD</sub> = V <sub>DD</sub> Max
V <sub>IHC</sub>	Input High Voltage (CMOS)	V <sub>DD</sub> -0.3		V	V <sub>DD</sub> = V <sub>DD</sub> Max
V <sub>OL</sub>	Output Low Voltage		0.2	V	I <sub>OL</sub> = 100μA, V <sub>DD</sub> = V <sub>DD</sub> Min
V <sub>OH</sub>	Output High Voltage	V <sub>DD</sub> -0.2		V	I <sub>OH</sub> = -100 μA, V <sub>DD</sub> = V <sub>DD</sub> Min
I <sub>H</sub>	Supervoltage Current for A <sub>9</sub> for Read-ID		200	μA	CE# = OE# = V <sub>IL</sub> , A <sub>9</sub> = V <sub>H</sub> Max.

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**TABLE 5: PROGRAM/ERASE DC OPERATING CHARACTERISTICS**  
 $V_{DD} = 2.7 \text{ to } 3.6\text{V}$ ,  $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I <sub>DD</sub>	V <sub>DD</sub> Erase or Program Current		30	mA	CE# = V <sub>IL</sub> , OE# = V <sub>H</sub> , V <sub>DD</sub> = V <sub>DD</sub> Max, WE# = V <sub>IL</sub>
I <sub>LI</sub>	Input Leakage Current		1	μA	V <sub>IN</sub> = GND to V <sub>DD</sub> , V <sub>DD</sub> = V <sub>DD</sub> Max
I <sub>LO</sub>	Output Leakage Current		1	μA	V <sub>OUT</sub> = GND to V <sub>DD</sub> , V <sub>DD</sub> = V <sub>DD</sub> Max
V <sub>H</sub>	Supervoltage for A <sub>9</sub> and OE#	11.4	12.6	V	
I <sub>H</sub>	Supervoltage Current for A <sub>9</sub> and OE#		200	μA	OE# = V <sub>H</sub> Max, A <sub>9</sub> = V <sub>H</sub> Max, V <sub>DD</sub> = V <sub>DD</sub> Max, CE# = V <sub>IL</sub>

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**TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS**

Symbol	Parameter	Minimum	Units
T <sub>PU-READ</sub>	Power-up to Read Operation	100	μs
T <sub>PU-WRITE</sub>	Power-up to Write Operation	100	μs

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**TABLE 7: CAPACITANCE (T<sub>A</sub> = 25 °C, f=1 MHz, other pins open)**

Parameter	Description	Test Condition	Maximum
C <sub>I/O</sub> <sup>(1)</sup>	I/O Pin Capacitance	V <sub>I/O</sub> = 0V	12 pF
C <sub>IN</sub> <sup>(1)</sup>	Input Capacitance	V <sub>IN</sub> = 0V	6 pF

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**Note:** <sup>(1)</sup>This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 8: RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Minimum Specification	Units	Test Method
N <sub>END</sub>	Endurance	1000	Cycles	JEDEC Standard A117
T <sub>DR</sub> <sup>(1)</sup>	Data Retention	100	Years	JEDEC Standard A103
V <sub>ZAP_HBM</sub> <sup>(1)</sup>	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
V <sub>ZAP_MM</sub> <sup>(1)</sup>	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I <sub>LTH</sub> <sup>(1)</sup>	Latch Up	100 + I <sub>DD</sub>	mA	JEDEC Standard 78

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**Note:** <sup>(1)</sup> This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



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### AC CHARACTERISTICS

**TABLE 9: READ CYCLE TIMING PARAMETERS**  
 $V_{DD} = 2.7 \text{ to } 3.6\text{V}$ ,  $T_A = 0^\circ\text{C to } 70^\circ\text{C}$  (Commercial)

Symbol	Parameter	SST37VF512-70 SST37VF010-70 SST37VF020-70 SST37VF040-70		SST37VF512-90 SST37VF010-90 SST37VF020-90 SST37VF040-90		Units
		Min	Max	Min	Max	
T <sub>RC</sub>	Read Cycle Time	70		90		ns
T <sub>CE</sub>	Chip Enable Access Time		70		90	ns
T <sub>AA</sub>	Address Access Time		70		90	ns
T <sub>OE</sub>	Output Enable Access Time		35		45	ns
T <sub>CLZ</sub>	CE# Low to Active Output	0		0		ns
T <sub>OLZ</sub>	OE# Low to Active Output	0		0		ns
T <sub>CHZ</sub>	CE# High to High-Z Output		30		30	ns
T <sub>OHZ</sub>	OE# High to High-Z Output		30		30	ns
T <sub>OH</sub>	Output Hold from Address Change	0		0		ns

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**TABLE 10: PROGRAM/ERASE CYCLE TIMING PARAMETERS**  
 $V_{DD} = 2.7 \text{ to } 3.6\text{V}$ ,  $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$

Symbol	Parameter	Min	Max	Units
T <sub>PC</sub>	Program Cycle Time	12		μs
T <sub>CES</sub>	CE# Setup Time	1		μs
T <sub>CEH</sub>	CE# Hold Time	1		μs
T <sub>AS</sub>	Address Setup Time	1		μs
T <sub>AH</sub>	Address Hold Time	1		μs
T <sub>DS</sub>	Data Setup Time	1		μs
T <sub>DH</sub>	Data Hold Time	1		μs
T <sub>PRT</sub>	OE# Rise Time for Program and Erase	1		μs
T <sub>VPS</sub>	OE# Setup Time for Program and Erase	1		μs
T <sub>VPH</sub>	OE# Hold Time for Program and Erase	1		μs
T <sub>PW</sub>	WE# Program Pulse Width	10	15	μs
T <sub>EW</sub>	WE# Erase Pulse Width	100	500	ms
T <sub>VR</sub>	OE#/A <sub>9</sub> Recovery Time for Erase	1		μs
T <sub>ART</sub>	A <sub>9</sub> Rise Time to 12V during Erase	1		μs
T <sub>A9S</sub>	A <sub>9</sub> Setup Time during Erase	1		μs
T <sub>A9H</sub>	A <sub>9</sub> Hold Time during Erase	1		μs

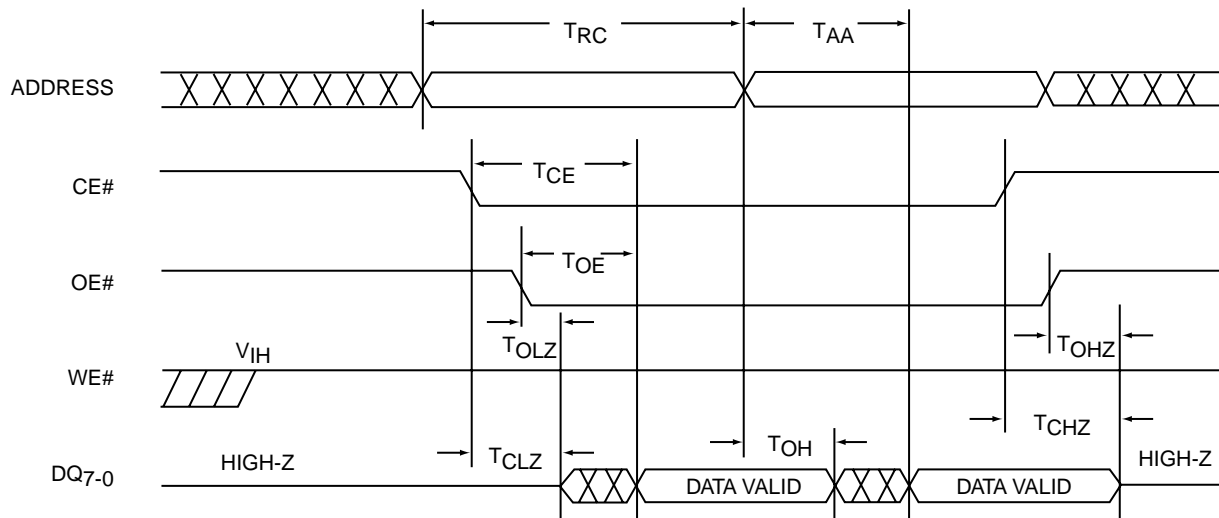
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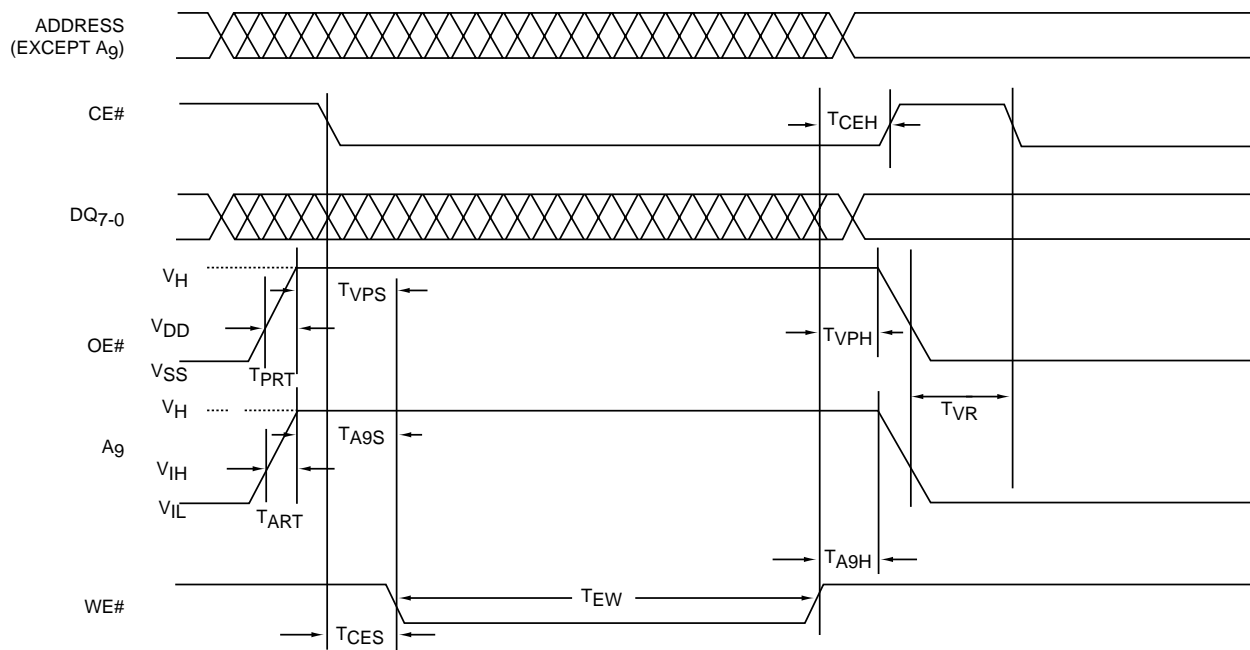
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**FIGURE 4: READ CYCLE TIMING DIAGRAM**



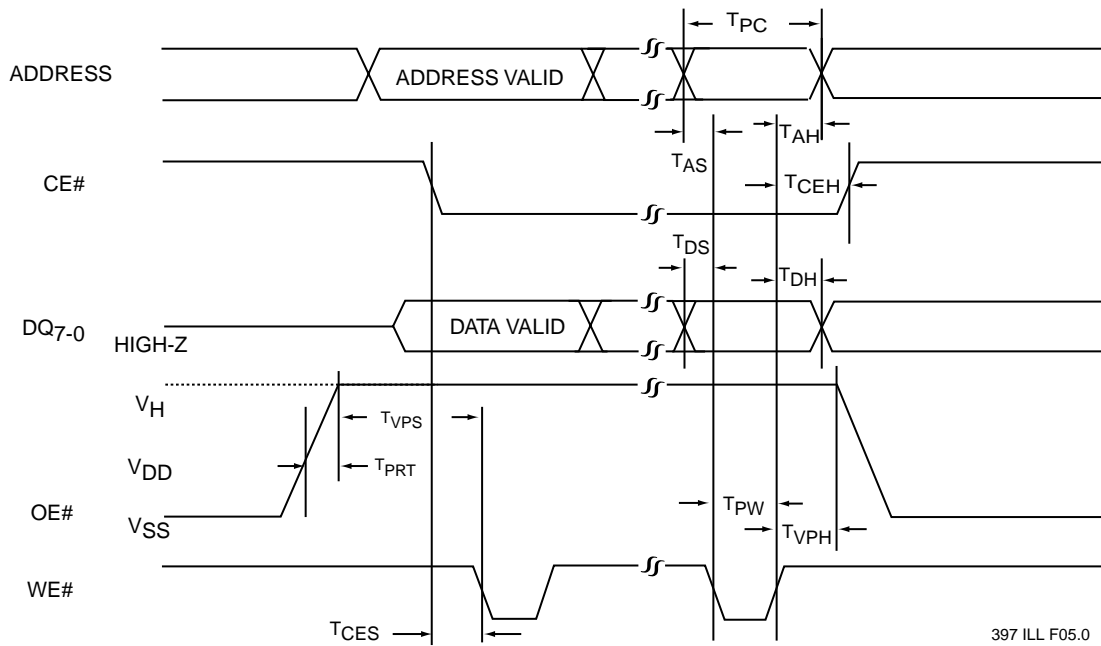
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**FIGURE 5: CHIP-ERASE TIMING DIAGRAM**



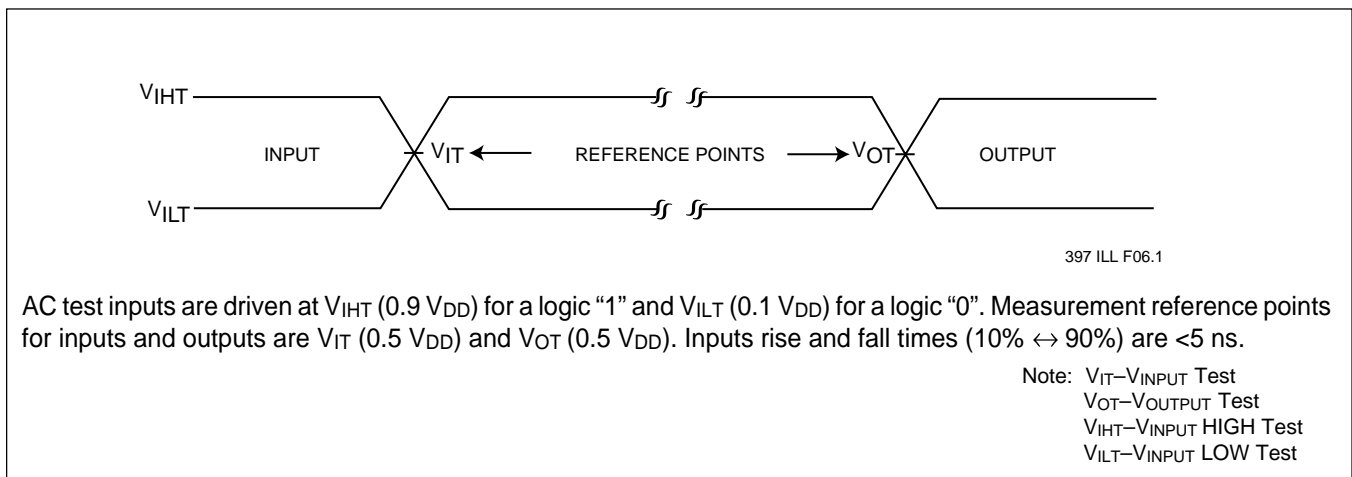
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FIGURE 6: BYTE-PROGRAM TIMING DIAGRAM



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AC test inputs are driven at  $V_{IHT}$  ( $0.9 V_{DD}$ ) for a logic "1" and  $V_{ILT}$  ( $0.1 V_{DD}$ ) for a logic "0". Measurement reference points for inputs and outputs are  $V_{IT}$  ( $0.5 V_{DD}$ ) and  $V_{OT}$  ( $0.5 V_{DD}$ ). Inputs rise and fall times ( $10\% \leftrightarrow 90\%$ ) are  $<5$  ns.

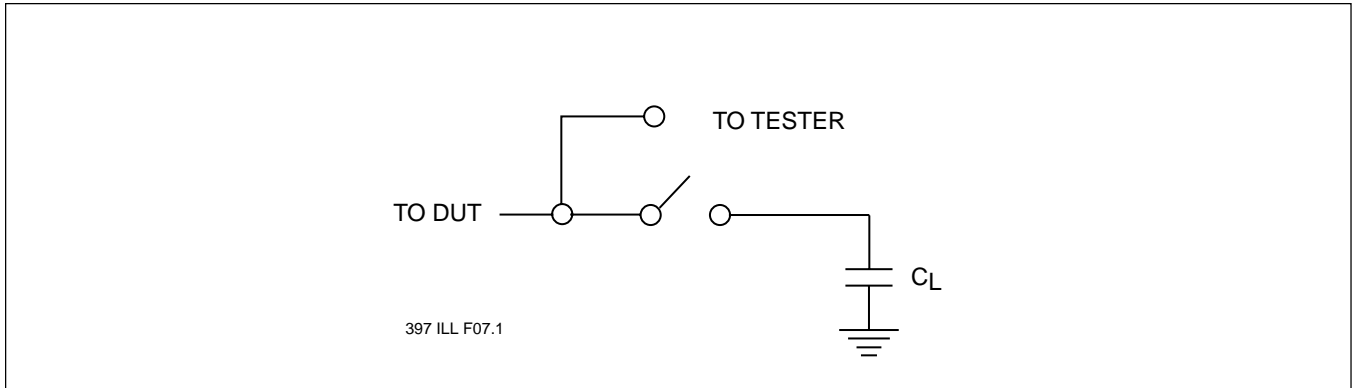
Note:  $V_{IT}$ - $V_{INPUT}$  Test  
 $V_{OT}$ - $V_{OUTPUT}$  Test  
 $V_{IHT}$ - $V_{INPUT}$  HIGH Test  
 $V_{ILT}$ - $V_{INPUT}$  LOW Test

FIGURE 7: AC INPUT/OUTPUT REFERENCE WAVEFORMS

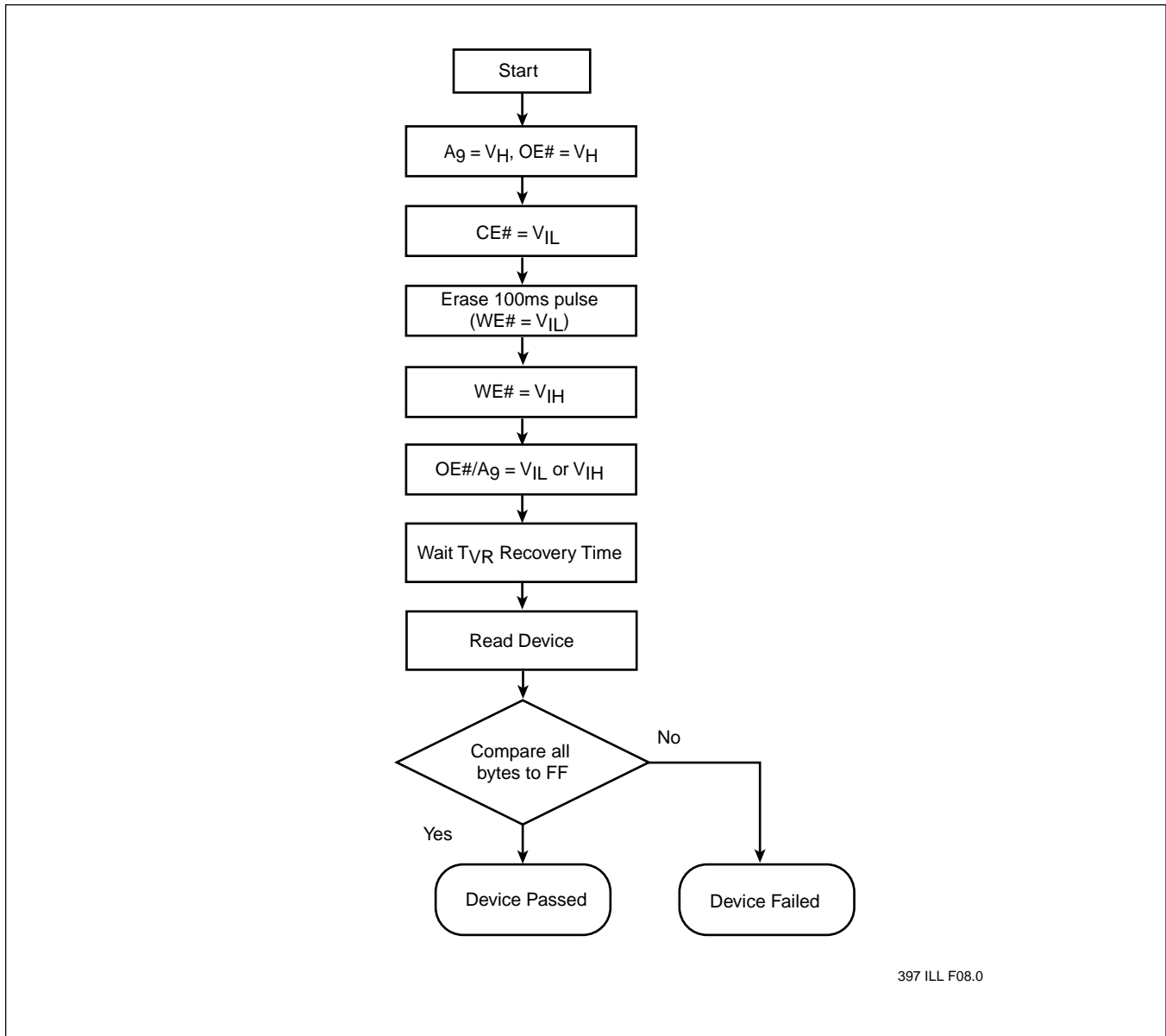
**512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Many-Time Programmable Flash  
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**FIGURE 8: A TEST LOAD EXAMPLE**



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FIGURE 9: CHIP-ERASE ALGORITHM



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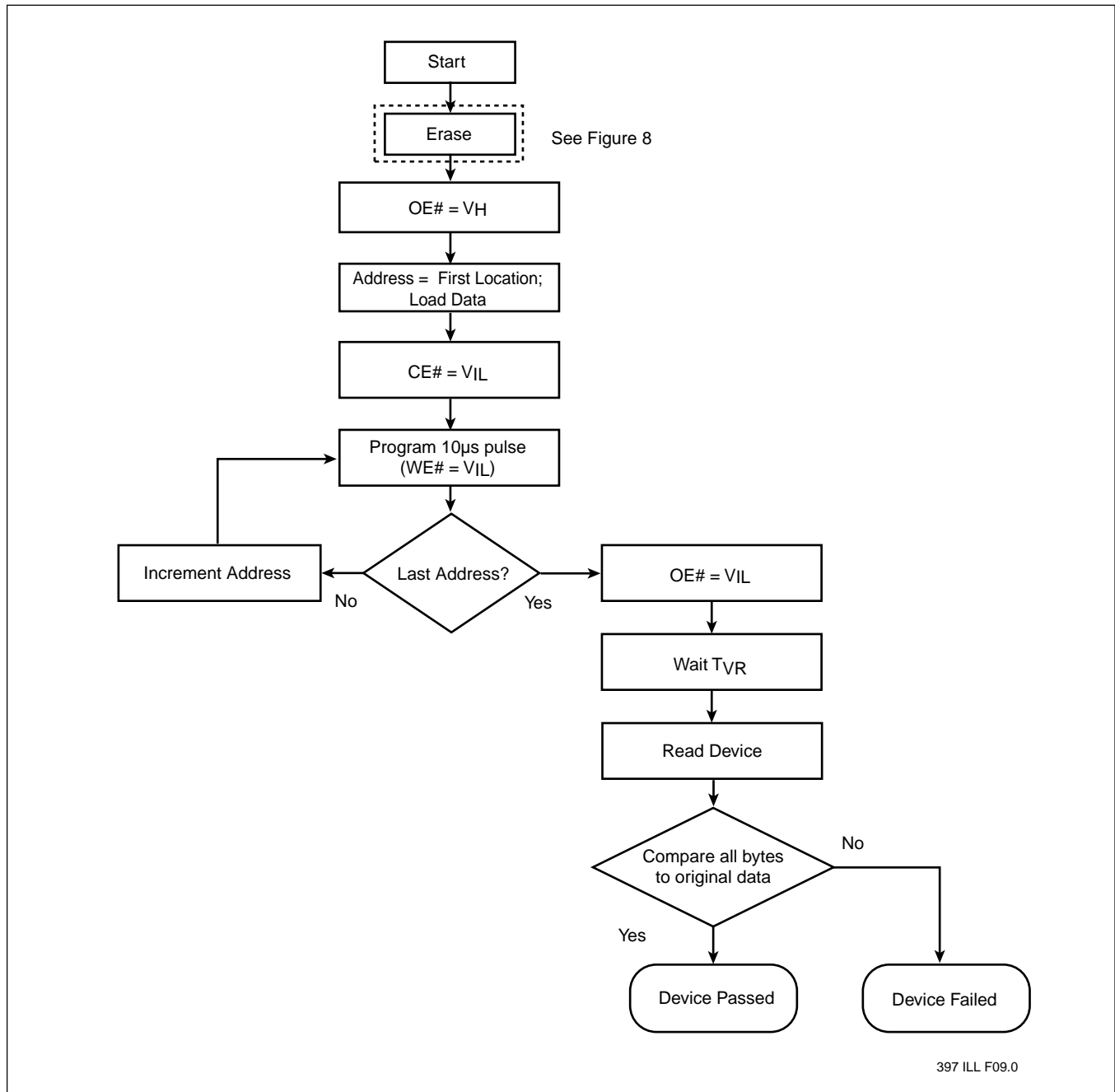


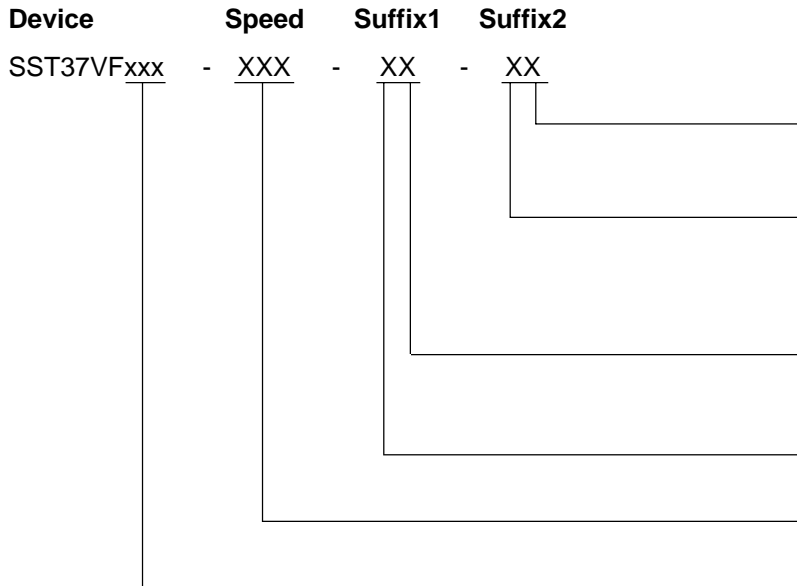
FIGURE 10: BYTE-PROGRAM ALGORITHM



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## PRODUCT ORDERING INFORMATION



### Package Modifier

H = 32 pins  
Numeric = Die modifier

### Package Type

P = PDIP  
N = PLCC  
W = TSOP 8mm x14mm

### Operating Temperature

C = Commercial = 0° to 70°C  
I = Industrial = -40° to 85°C

### Minimum Endurance

3 = 1000 cycles

### Read Access Speed

70 = 70 ns, 90 = 90 ns

### Device Density

512 = 512 Kilobit  
010 = 1 Megabit  
020 = 2 Megabit  
040 = 4 Megabit

### SST37VF512 Valid combinations

SST37VF512-70-3C-WH	SST37VF512-70-3C-NH	
SST37VF512-90-3C-WH	SST37VF512-90-3C-NH	SST37VF512-90-3C-PH
SST37VF512-70-3I-WH	SST37VF512-70-3I-NH	
SST37VF512-90-3I-WH	SST37VF512-90-3I-NH	

### SST37VF010 Valid combinations

SST37VF010-70-3C-WH	SST37VF010-70-3C-NH	
SST37VF010-90-3C-WH	SST37VF010-90-3C-NH	SST37VF010-90-3C-PH
SST37VF010-70-3I-WH	SST37VF010-70-3I-NH	
SST37VF010-90-3I-WH	SST37VF010-90-3I-NH	

### SST37VF020 Valid combinations

SST37VF020-70-3C-WH	SST37VF020-70-3C-NH	
SST37VF020-90-3C-WH	SST37VF020-90-3C-NH	SST37VF020-90-3C-PH
SST37VF020-70-3I-WH	SST37VF020-70-3I-NH	
SST37VF020-90-3I-WH	SST37VF020-90-3I-NH	

### SST37VF040 Valid combinations

SST37VF040-70-3C-WH	SST37VF040-70-3C-NH	
SST37VF040-90-3C-WH	SST37VF040-90-3C-NH	SST37VF040-90-3C-PH
SST37VF040-70-3I-WH	SST37VF040-70-3I-NH	
SST37VF040-90-3I-WH	SST37VF040-90-3I-NH	

**Example:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

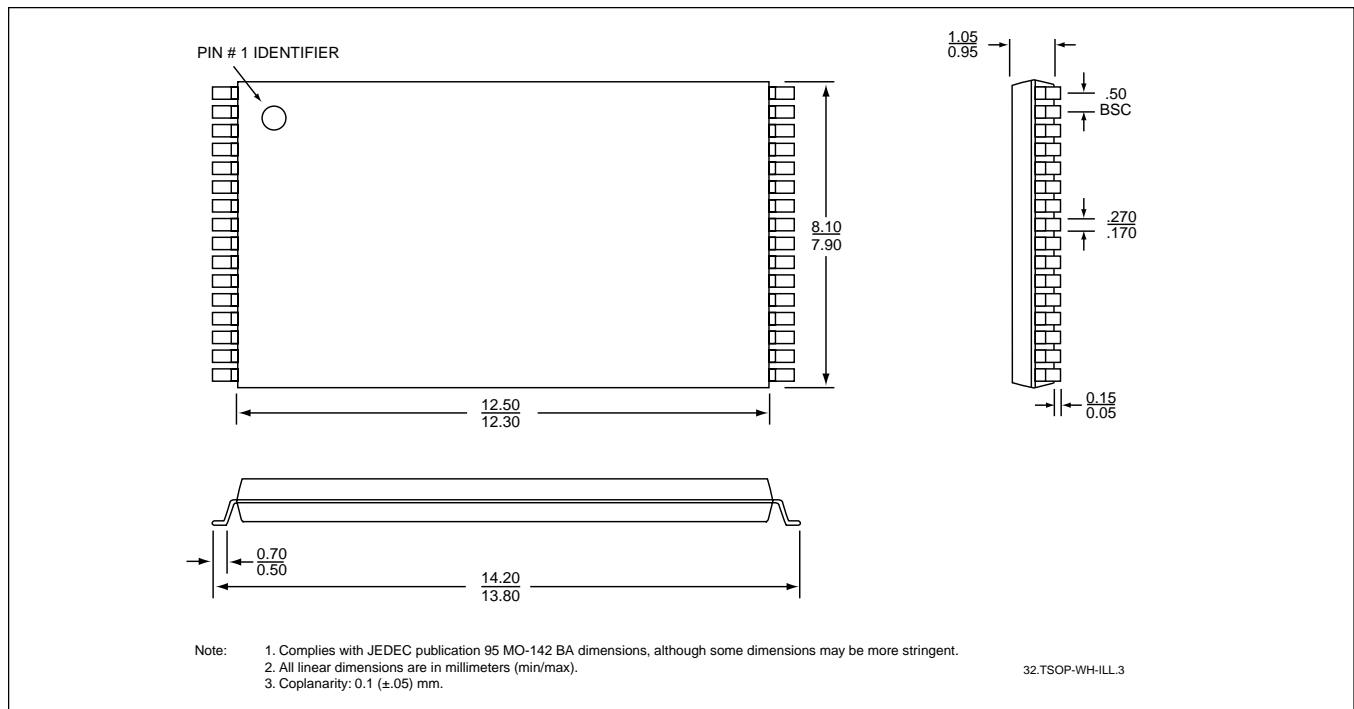


# 512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Many-Time Programmable Flash

## SST37VF512 / SST37VF010 / SST37VF020 / SST37VF040

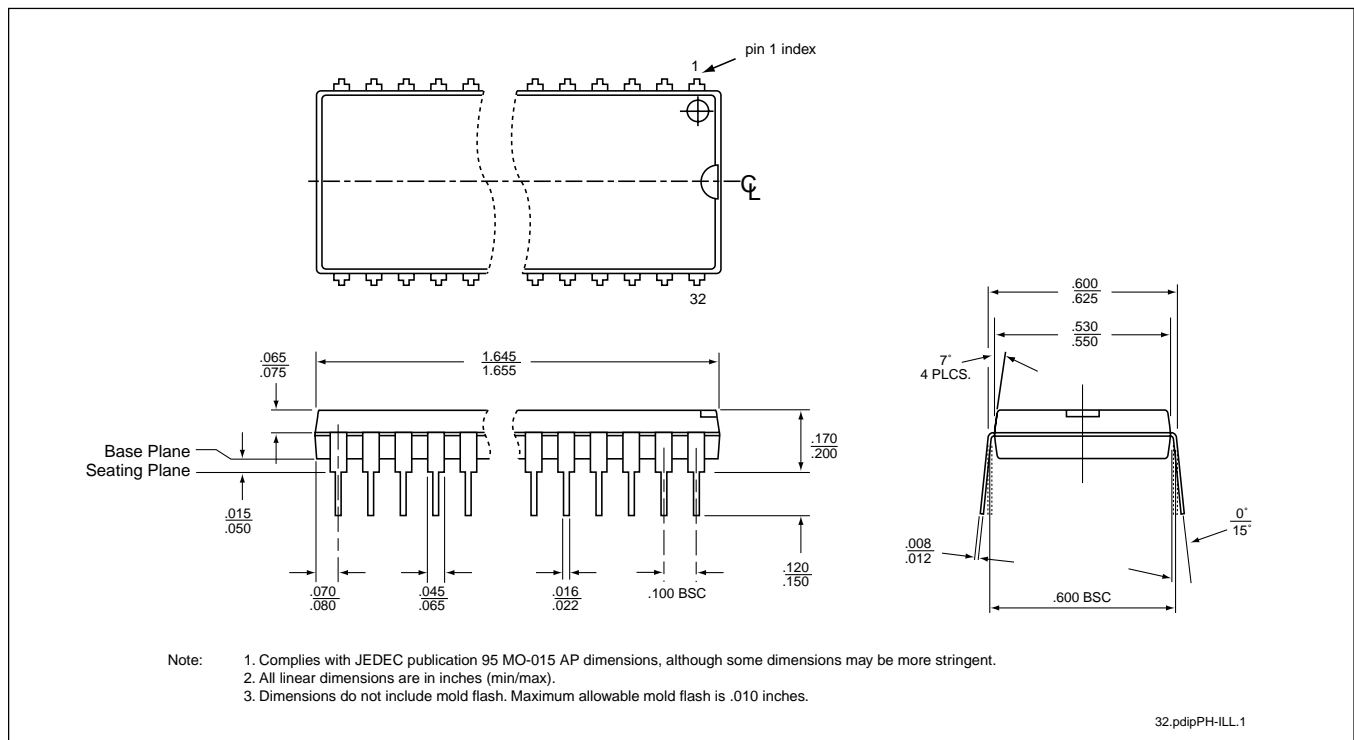
Data Sheet

### PACKAGING DIAGRAMS



### 32-PIN THIN SMALL OUTLINE PACKAGE (TSOP)

SST PACKAGE CODE: WH



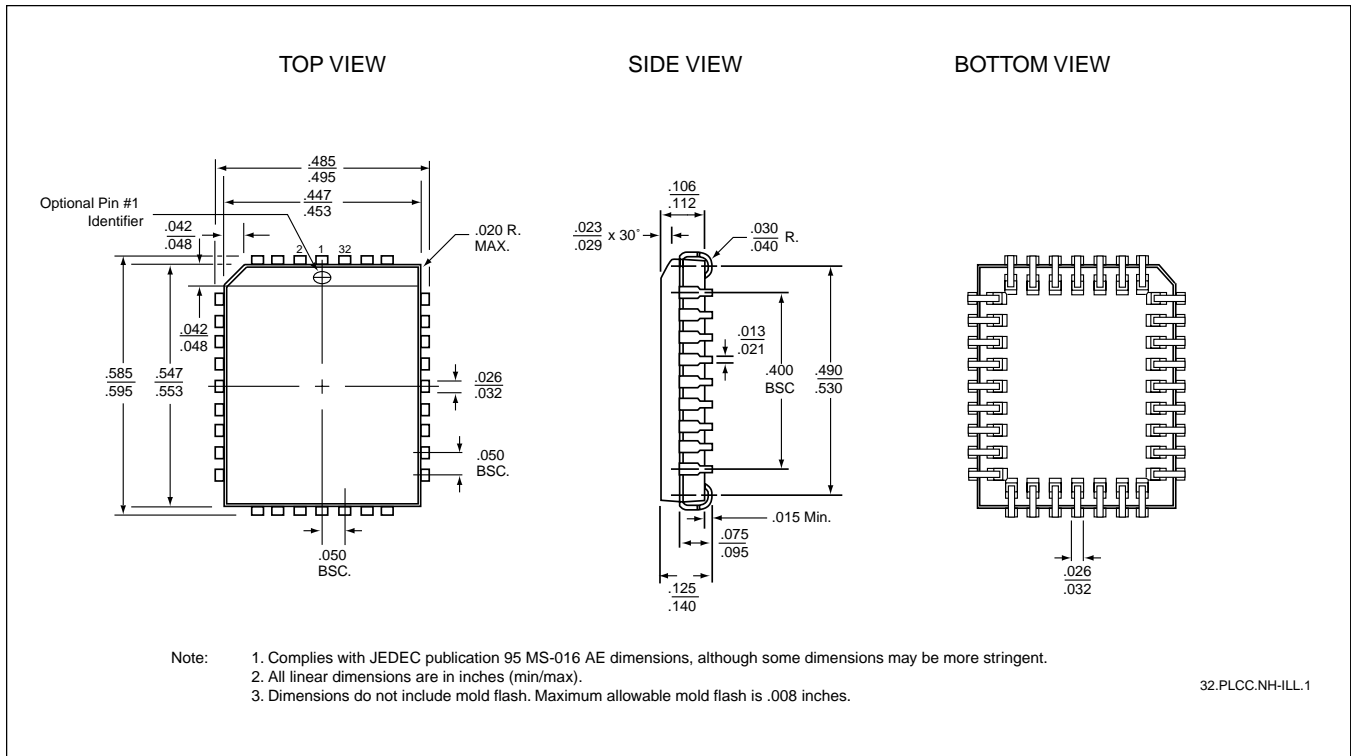
### 32-PIN PLASTIC DUAL-IN-LINE PACKAGE (PDIP)

SST PACKAGE CODE: PH



# 512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit Many-Time Programmable Flash SST37VF512 / SST37VF010 / SST37VF020 / SST37VF040

Data Sheet



**32-PIN PLASTIC LEAD CHIP CARRIER (PLCC)**  
**SST PACKAGE CODE: NH**