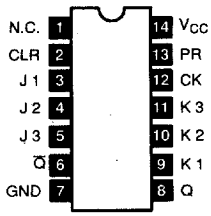
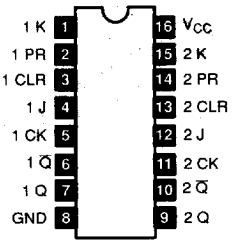
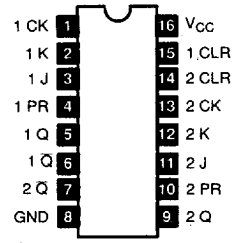
**NTE74110** 14–Lead DIP, See Diag. 247
AND Gated J–K Master/Slave Flip–Flop w/Data Lockout



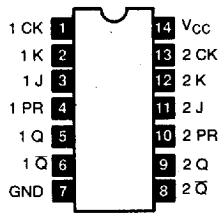

**NTE74111** 16–Lead DIP, See Diag. 249
Dual J–K Flip–Flop Master/Slave w/Data Lockout



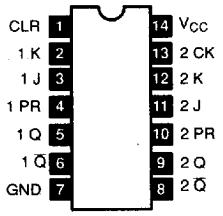

**NTE74LS112A, NTE74S112** 16–Lead DIP, See Diag. 249
Dual J–K Negative Edge Triggered Flip–Flop w/Preset & Clear



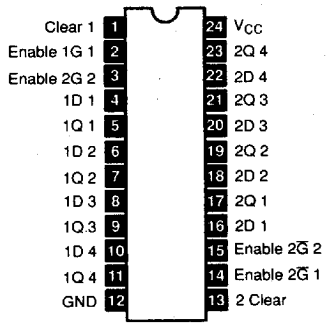

**NTE74LS113, NTE74S113** 14–Lead DIP, See Diag. 247
Dual J–K Negative Edge Triggered Flip–Flop w/Preset



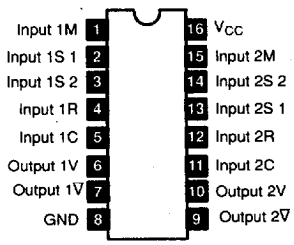

**NTE74LS114, NTE74S114** 14–Lead DIP, See Diag. 247
Dual J–K Negative Edge Triggered Flip–Flop w/Preset, Common Clock & Clear



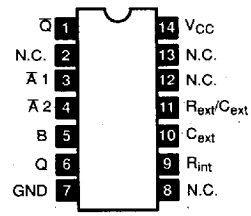

**NTE74116** 24–Lead DIP, See Diag. 252
Dual 4–Bit Latch



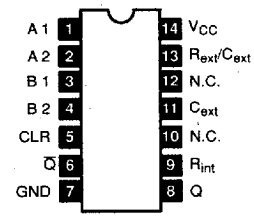

**NTE74120** 16–Lead DIP, See Diag. 249
Dual Pulse Synchronizer/Driver



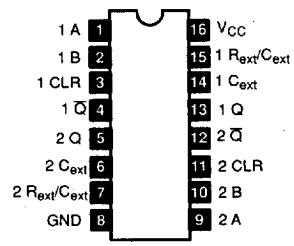

**NTE74121** 14–Lead DIP, See Diag. 247
Monostable Multivibrator




**NTE74122, NTE74LS122** 14–Lead DIP, See Diag. 247
Retriggerable Monostable Multivibrator w/Clear

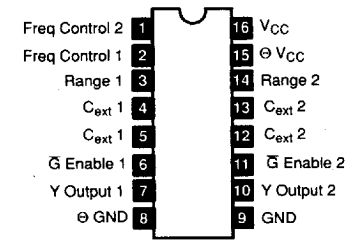



**NTE74123, NTE74HC123, NTE74LS123** 16–Lead DIP, See Diag. 249
Dual Retriggerable Monostable Multivibrator w/Clear

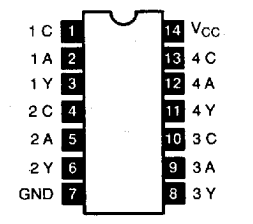



**Note:** For NTE74HC123 **ONLY**, See Diag. 248

**NTE74LS124, NTE74S124** 16–Lead DIP, See Diag. 249
Dual Voltage Controlled Oscillator




**NTE74125, NTE74HC125, NTE74LS125A** 14–Lead DIP, See Diag. 247
Quad Bus Buffer w/3–State Outputs




See Diagrams, beginning on Page 1–293



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