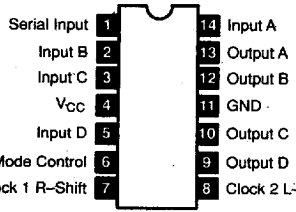
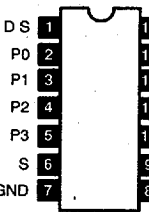
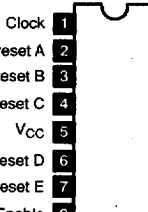
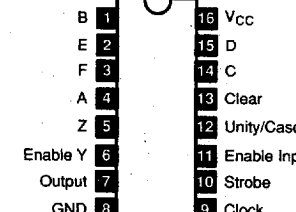
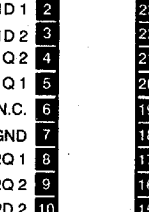
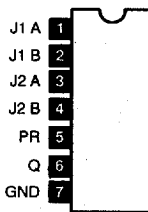
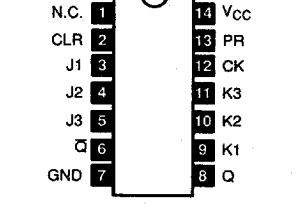
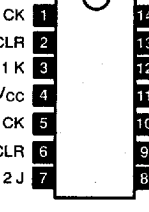
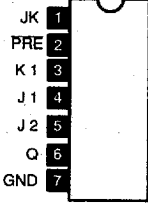
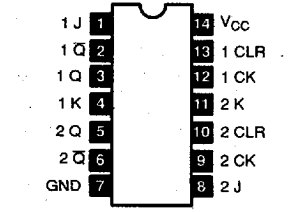
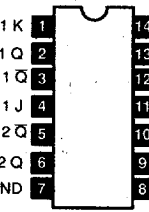
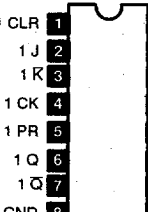


# INTEGRATED CIRCUITS - TTL

## (TRANSISTOR TRANSISTOR LOGIC)

<p><b>NTE74C95</b> 14-Lead DIP, See Diag. 247 4-Bit Parallel In/Parallel Out Shift Register</p>  <p>Serial Input 1, Input A 14, Input B 2, Output A 13, Input C 3, Output B 12, Vcc 4, GND 11, Input D 5, Output C 10, Mode Control 6, Output D 9, Clock 1 R-Shift 7, Clock 2 L-Shift 8</p>	<p><b>NTE74LS95B</b> 14-Lead DIP, See Diag. 247 4-Bit Shift Register</p>  <p>D S 1, Vcc 14, P0 2, Q0 13, P1 3, Q1 12, P2 4, Q2 11, P3 5, Q3 10, S 6, CP 1 9, GND 7, CP 2 8</p>	<p><b>NTE7496</b> 16-Lead DIP, See Diag. 249 5-Bit Shift Register w/Async Preset</p>  <p>Clock 1, Clear 16, Preset A 2, Output QA 15, Preset B 3, Output QB 14, Preset C 4, Output QC 13, Vcc 5, GND 12, Preset D 6, Output QD 11, Preset E 7, Output QE 10, Preset Enable 8, Serial Input 9</p>
<p><b>NTE7497</b> 16-Lead DIP, See Diag. 249 Synchronous 6-Bit Binary Rate Multiplier</p>  <p>B 1, Vcc 16, E 2, D 15, F 3, C 14, A 4, Clear 13, Z 5, Unity/Cascade 12, Enable Y 6, Enable Input 11, Output 7, Strobe 10, GND 8, Clock 9</p>	<p><b>NTE74100</b> 24-Lead DIP, See Diag. 252 8-Bit Bistable Latch</p>  <p>N.C. 1, Vcc 24, 1D 1 2, Enable 1G 23, 1D 2 3, 1D 3 22, 1Q 2 4, 1D 4 21, 1Q 1 5, 1Q 4 20, N.C. 6, 1Q 3 19, GND 7, 2Q 3 18, 2Q 1 8, 2Q 4 17, 2Q 2 9, 2D 4 16, 2D 2 10, 2D 3 15, 2D 1 11, N.C. 14, Enable 2G 12, N.C. 13</p>	<p><b>NTE74H101</b> 14-Lead DIP, See Diag. 247 AND/OR Gate J-K Negative Edge Triggered Flip-Flop w/Preset</p>  <p>J1 A 1, Vcc 14, J1 B 2, CK 13, J2 A 3, K2 B 12, J2 B 4, K2 A 11, PR 5, K1 B 10, Q 6, K1 A 9, GND 7, Q 8</p>
<p><b>NTE74H102</b> 14-Lead DIP, See Diag. 247 AND Gated J-K Negative Edge Triggered Flip-Flop w/Clear &amp; Preset</p>  <p>N.C. 1, Vcc 14, CLR 2, PR 13, J1 3, CK 12, J2 4, K3 11, J3 5, K2 10, Q 6, K1 9, GND 7, Q 8</p>	<p><b>NTE74H103</b> 14-Lead DIP, See Diag. 247 Dual J-K Negative Edge Triggered Flip-Flop w/Clears</p>  <p>1 CK 1, 1 J 14, 1 CLR 2, 1 Q 13, 1 K 3, 1 Q 12, Vcc 4, 11 GND, 2 CK 5, 2 K 10, 2 CLR 6, 2 Q 9, 2 J 7, 2 Q 8</p>	<p><b>NTE74105</b> 14-Lead DIP, See Diag. 247 Gated J-K Master-Slave Flip-Flop</p>  <p>JK 1, Vcc 14, PRE 2, CLR 13, K 1 3, J 3 12, J 1 4, K 3 11, J 2 5, K 2 10, Q 6, CLK 9, GND 7, Q 8</p>
<p><b>NTE74107, NTE74C107, NTE74LS107</b> 14-Lead DIP, See Diag. 247 Dual J-K Negative Edge Triggered Flip-Flop w/Clear</p>  <p>1 J 1, Vcc 14, 1 Q 2, 1 CLR 13, 1 Q 3, 1 CK 12, 1 K 4, 2 K 11, 2 Q 5, 2 CLR 10, 2 Q 6, 2 CK 9, GND 7, 2 J 8</p>	<p><b>NTE74H108</b> 14-Lead DIP, See Diag. 247 Dual J-K Negative Edge Triggered Flip-Flop w/Presets, Common Clear, &amp; Common Clock</p>  <p>1 K 1, Vcc 14, 1 Q 2, 1 PR 13, 1 Q 3, 12 CLR 14, 1 J 4, 11 2 J, 2 Q 5, 10 2 PR, 2 Q 6, 9 CK, GND 7, 8 2 K</p>	<p><b>NTE74109, NTE74HC109, NTE74LS109A</b> 16-Lead DIP, See Diag. 249 Dual J-K Positive Edge Triggered Flip-Flop w/Clear &amp; Preset</p>  <p>1 CLR 1, Vcc 16, 1 J 2, 15 2 CLR, 1 K 3, 14 2 J, 1 CK 4, 13 2 K, 1 PR 5, 12 2 CK, 1 Q 6, 11 2 PR, 1 Q 7, 10 2 Q, GND 8, 9 2 Q</p>

See Diagrams, beginning on Page 1-293

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