Agilent HFBR-5730L/LP Small Form Factor Pluggable Optical Transceiver for Fibre Channel (1.0625 GBd)

Data Sheet

Description

The HFBR-5730L optical transceiver from Agilent Technologies offers maximum flexibility to Fibre Channel designers, manufacturers, and system integrators to implement a range of solutions for multimode Fibre Channel applications. In order to provide a wide range of system level performance, this product is fully compliant with all equipment meeting the new Fibre Channel FC-PI 100-M5-SN-I and 100-M6-SN-I 1.0625 GBd specifications, and is also compliant with the older Fibre Channel FC-PH-2 100-M5-SN-I, and the FC-PH-2 100-M6-SN-I 1.0625 GBd specifications.

Module Package

The transceiver meets the Small Form Pluggable (SFP) industry standard package utilizing an integral LC-Duplex optical interface connector. The hot-pluggable capability of the SFP package allows the module to be installed at any time – even with the host system operating and on-line. This allows for system configuration changes or maintenance without system down time.

Features

- **Compliant with 1.0625 GBd Fibre Channel FC-1 standard**
  - **– FC-PI 100-M5-SN-I for 50/120 μm multimode cables**
  - **– FC-PI 100-M6-SN-I for 62.5/125 μm multimode cables**
- **Compliant with Fibre Channel FC-PH-2 standard**
- **Industry standard Small Form Pluggable (SFP) package**
- **LC-Duplex connector optical interface**
- **Link lengths at 1.0625 GBd: 0.5 to 500 m – 50/125 μm MMF 0.5 to 300 m – 62.5/125 μm MMF**
- **Reliable 850 nm Vertical Cavity Surface Emitting Laser (VCSEL) source technology**
- **Laser AEL Class I (eye safe) per: US 21 CFR (J) EN 60825-1 (+ AII)**
- **Single +3.3 V power supply operation**
- **Hot pluggable**
- **Delatch options:**
  - **– HFBR-5730L standard delatch**
  - **– HFBR-5730LP bail-wire pull delatch**

Applications

- **Mass storage system I/O**
- **Computer system I/O**
- **High-speed peripheral interface**
- **High-speed switching systems**
- **Host adapter I/O**
- **RAID cabinets**

Related Products

- **HFBR-5720L: 2.125/1.0625 GBd 3.3 V SFP Fibre Channel Transceiver for FC-PI-2**
- **HFBR-5921L: 2.125/1.0625 GBd 3.3 V SFF PTH Fibre Channel Transceiver for FC-PI-2**
- **HFBR-5710L: 850 nm 1.25 GBd 3.3 V SFP Gigabit Ethernet Transceiver**
- **HFBR-53A3VEM/VFM: 850 nm 1.0625 GBd 3 V, 1 x 9 Fibre Channel Transceiver for FC-PH-2**
- **HFBR-5602: 850 nm 5 V Gigabit Interface Converter (GBIC) for Fibre Channel FC-PH-2 for FC-PH2**
- **HDMP-2630/2631 2.125/1.0625 GBd TRx family of SerDes IC**
- **HDMP-1687 1.0625 GBd Quad SerDes IC**

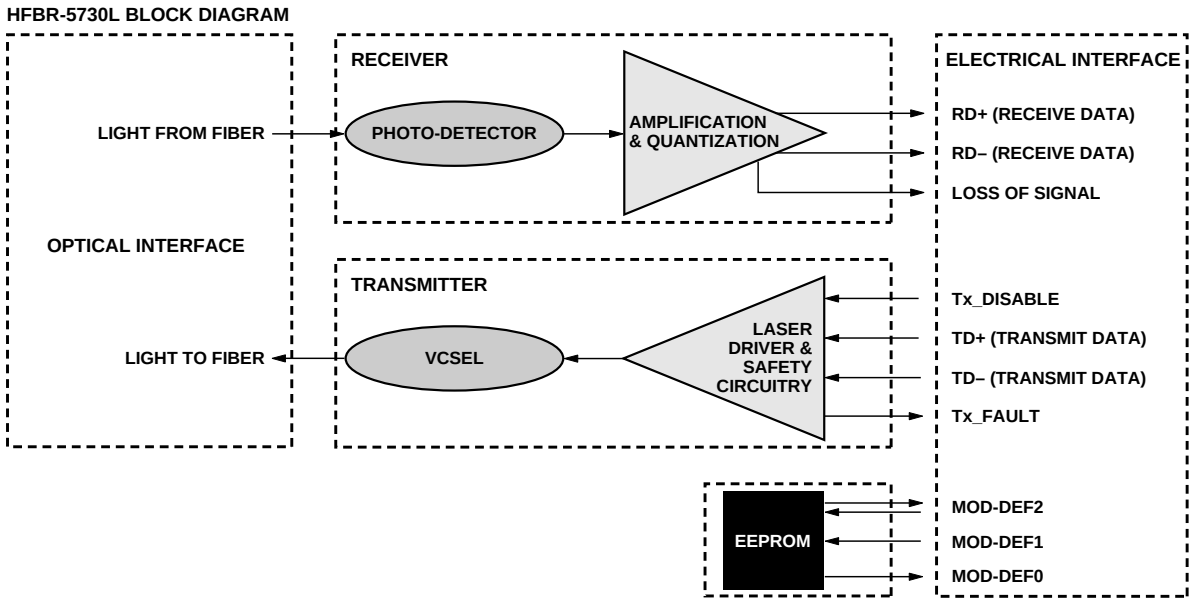


Figure 1. Transceiver functional diagram.

The HFBR-5730L uses a reliable 850 nm VCSEL source and requires a 3.3 V DC power supply for optimal system design.

Module Diagrams

Figure 1 illustrates the major functional components of the HFBR-5730L. The connection diagram of the module is shown in Figure 2. Figure 7 depicts the external configuration and dimensions of the module.

Installation

The HFBR-5730L can be installed in or removed from any MultiSource Agreement (MSA) compliant Small Form Pluggable port regardless of whether the host equipment is operating or not. The module is simply inserted, electrical-interface first, under finger-pressure. Controlled hot-plugging is ensured by design and by 3-stage pin sequencing at the electrical interface. The module housing makes initial contact with the host board EMI shield mitigating potential damage due to Electro-Static Discharge (ESD). The 3-stage pin contact sequencing involves (1) Ground, (2) Power, and then (3) Signal pins, making contact with the host board surface mount connector in that order. This printed circuit board card-edge connector is depicted in Figure 2.

Serial Identification (EEPROM)

The HFBR-5730L complies with an industry standard MultiSource Agreement that defines the serial identification protocol. This protocol uses the 2-wire serial CMOS E2PROM protocol of the ATMEL AT24C01A or equivalent. The contents of the HFBR-5730L serial ID memory are defined in Table 10 as specified in the SFP MSA.

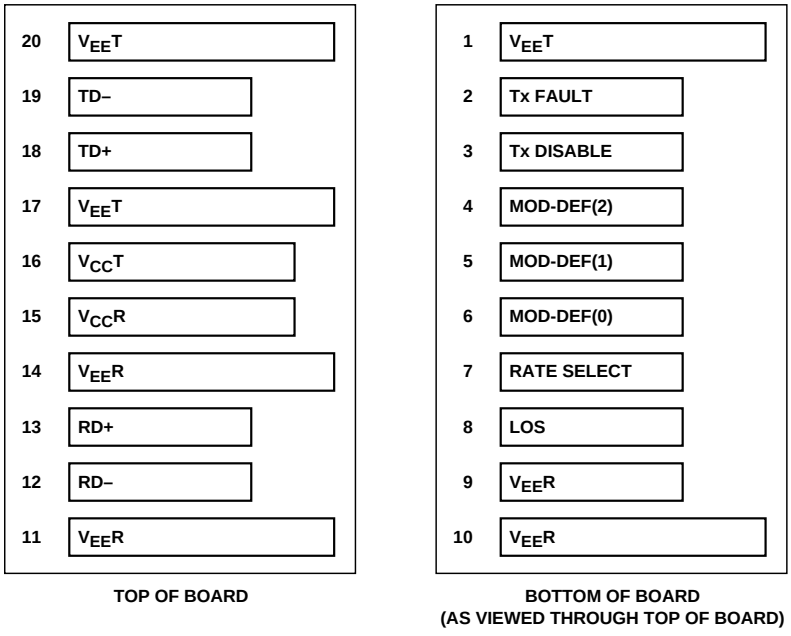


Figure 2. Connection diagram of module printed circuit board.

Transmitter Section

The transmitter section includes the transmitter optical subassembly (TOSA) and laser driver circuitry. The TOSA, containing an 850 nm VCSEL (Vertical Cavity Surface Emitting Laser) light source, is located at the optical interface and mates with the LC optical connector. The TOSA is driven by a custom silicon IC, which converts differential logic signals into an analog laser diode drive current. This Tx driver circuit regulates the optical power at a constant level provided the data pattern is valid 8B/10B DC balanced code.

Tx Disable

The HFBR-5730L accepts a transmit disable control signal input which shuts down the transmitter. A high signal implements this function while a low signal allows normal laser operation. In the event of a fault (e.g., eye safety circuit activated), cycling this control signal resets the module as depicted in Figure 6. The Tx Disable control should be actuated upon initialization of the module.

Tx Fault

The HFBR-5730L module features a transmit fault control signal output which when high indicates a laser transmit fault has occurred and when low indicates normal laser operation. A transmitter fault condition can be caused by deviations from the recommended module operating conditions or by violation of eye safety conditions. A transient fault can be cleared by cycling the Tx Disable control input.

Eye Safety Circuit

For an optical transmitter device to be eye-safe in the event of a single fault failure, the transmitter will either maintain normal, eye-safe operation or be disabled. In the event of an eye-safety fault, the VCSEL will be disabled.

Receiver Section

The receiver section includes the receiver optical subassembly (ROSA) and amplification/quantization circuitry. The ROSA, containing a PIN photodiode and custom transimpedance preamplifier, is located at the optical interface and mates with the LC optical connector. The ROSA is mated to a custom IC that provides post-amplification and quantization. This circuit also includes a loss of signal (LOS) detection circuit which provides an open collector logic high output in the absence of a usable input optical signal level.

Loss of Signal

The Loss of Signal (LOS) output signal indicates that the optical input signal to the receiver does not meet the minimum detectable level for Fibre Channel compliant signals. When LOS is high it indicates loss of signal. When LOS is low it indicates normal operation. The Loss Of Signal thresholds are set to indicate a definite optical fault has occurred (e.g., disconnected or broken fiber connection to receiver, failed transmitter).

Functional Data I/O

Agilent's HFBR-5730L fiber-optic transceiver is designed to accept industry standard differential signals. In order to reduce the number of passive components required on the customer's board, Agilent has included the functionality of the transmitter bias resistors and coupling capacitors within the fiber optic module. The transceiver is compatible with an "AC-coupled" configuration and is internally terminated. Figure 1 depicts the functional diagram of the HFBR 5730L. Caution should be taken to account for the proper interconnection between the supporting physical layer integrated circuits and the HFBR-5730L. Figure 4 illustrates the recommended interface circuit.

Several MSA compliant control data signals are implemented in the module and are depicted in Figure 6.

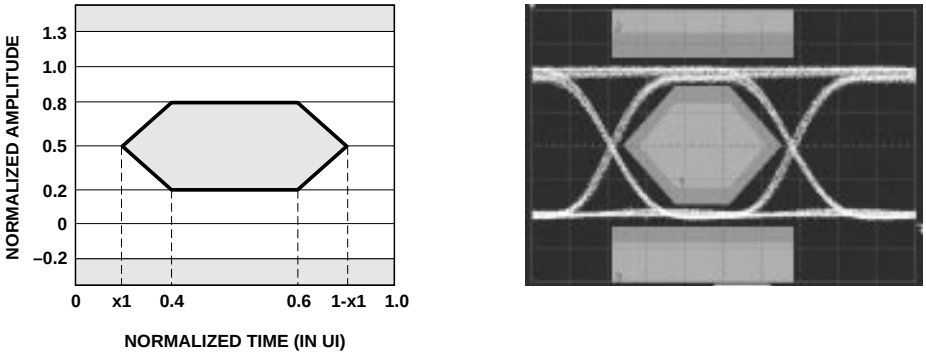


Figure 3. Transmitter eye mask diagram and typical transmitter eye.

Application Support

Evaluation Kit

To help you in your preliminary transceiver evaluation, Agilent offers a 1.0625 GBd Fibre Channel evaluation board. This board will allow testing of the fiber-optic VCSEL transceiver. Please contact your local Field Sales representative and request part number HFBR-0571.

Reference Designs

Reference designs for the HFBR-5730L fiber-optic transceiver and the HDMP-1687 physical layer IC are available to assist the equipment designer. Figure 4 depicts a typical application configuration, while Figure 5 depicts the MSA power supply filter circuit design. All artwork is available at the Agilent electronic bulletin board. Please contact your local Field Sales engineer for more information regarding application tools.

Regulatory Compliance

See Table 1 for transceiver Regulatory Compliance performance. The overall equipment design will determine the certification level. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

There are two conditions in which immunity to ESD damage is important. Table 1 documents our immunity to both of these conditions. The first condition is during handling of the transceiver prior to insertion into the transceiver port. To protect the transceiver, it is important to use normal ESD handling precautions. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas. The ESD sensitivity of the HFBR-5730L is compatible with typical industry production environments. The second condition is static discharges to the exterior of the host equipment chassis after installation. To the extent that the duplex LC optical interface is exposed to the outside of the host equipment chassis, it may be subject to system-level ESD requirements. The ESD performance of the HFBR-5730L exceeds typical industry standards.

Immunity

Equipment hosting the HFBR-5730L modules will be subjected to radio-frequency electromagnetic fields in some environments. The transceivers have good immunity to such fields due to their shielded design.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Agilent Technologies will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

The metal housing and shielded design of the HFBR-5730L minimize the EMI challenge facing the host equipment designer. These transceivers provide superior EMI performance. This greatly assists the designer in the management of the overall system EMI performance.

Eye Safety

These 850 nm VCSEL-based transceivers provide Class 1 eye safety by design. Agilent Technologies has tested the transceiver design for compliance with the requirements listed in Table 1: Regulatory Compliance, under normal operating conditions and under a single-fault condition.

Flammability

The HFBR-5730L VCSEL transceiver housing is made of metal and high strength, heat resistant, chemically resistant, and UL 94V-0 flame retardant plastic.

Caution

There are no user serviceable parts nor any maintenance required for the HFBR-5730L. Tampering with or modifying the performance of the HFBR-5730L will result in voided product warranty. It may also result in improper operation of the HFBR-5730L circuitry, and possible overstress of the laser source. Device degradation or product failure may result. Connection of the HFBR-5730L to a non-approved optical source, operating above the recommended absolute maximum conditions or operating the HFBR-5730L in a manner inconsistent with its design and function may result in hazardous radiation exposure and may be considered an act of modifying or manufacturing a laser product. The person(s) performing such an act is required by law to re-certify and re-identify the laser product under the provisions of U.S. 21 CFR (Subchapter J) and the TUV.

Ordering Information

Please contact your local field sales engineer or one of Agilent Technologies franchised distributors for ordering information. For technical information regarding this product, including the MSA, please visit Agilent Technologies Semiconductors Products Website at ***www.agilent.com/view/fiber***. Use the quick search feature to search for this part number. You may also contact Agilent Technologies Semiconductor Products Customer Response Center at 1-800-235-0312.

Table 1. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Class 2 (2000–3999 Volts)
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	Variation of IEC 61000-4-2	Typically withstand at least 25 kV without damage when the duplex LC connector receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22A) VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows a negligible effect from a 10 V/m field swept from 80 to 1000 MHz applied to the transceiver without a chassis enclosure.
Eye Safety	US FDA CDRH AEL Class 1 EN(IEC)60825-1,2, EN60950 Class 1	CDRH file # 9720151-13 TUV file # R2079009.5[1]
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment.	UL file # E173874

Note:

1. Changes to IEC 60825-1,2 are currently anticipated to allow higher eye-safe Optical Output Power levels. Agilent may choose to take advantage of these in future revisions to this part.

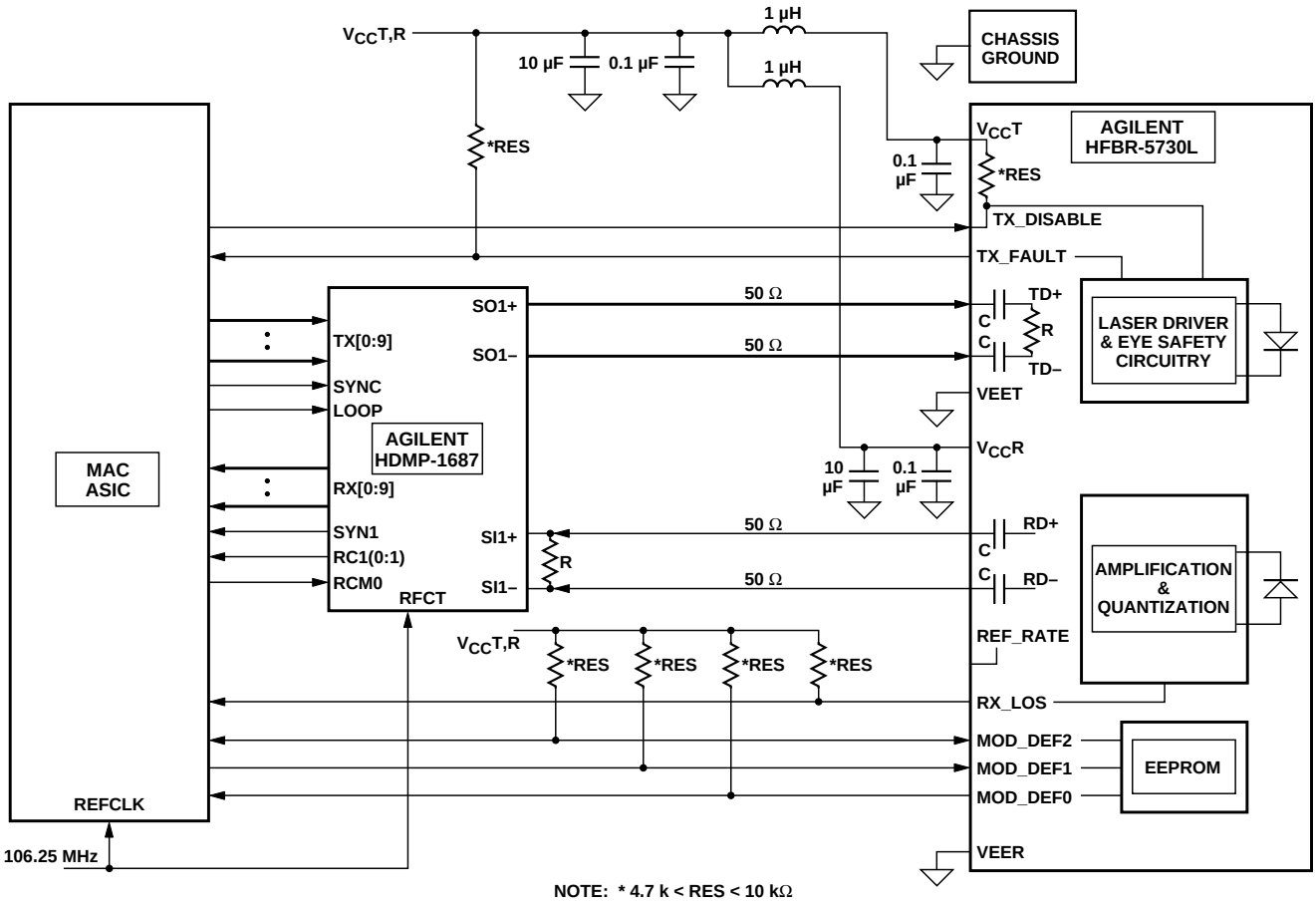
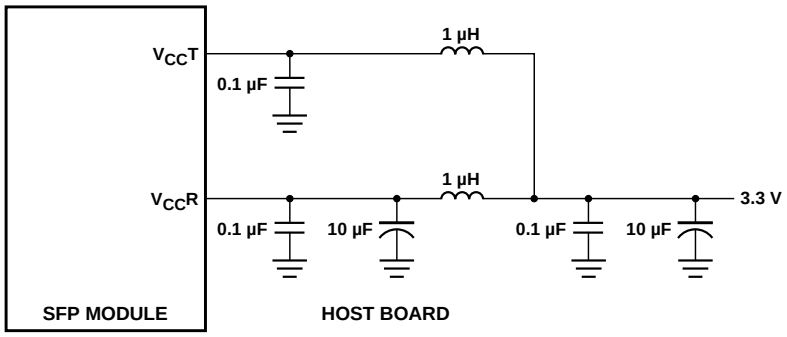


Figure 4. Typical application configuration.



NOTE: INDUCTORS MUST HAVE LESS THAN 1 Ω SERIES RESISTANCE PER MSA.

Figure 5. MSA recommended power supply filter.

Table 2. Pin Description

Pin	Name	Function/Description	MSA Notes
1	$V_{EE}T$	Transmitter Ground	
2	TX Fault	Transmitter Fault Indication – High indicates a fault	1
3	TX Disable	Transmitter Disable – Module disables on high or open	2
4	MOD-DEF2	Module Definition 2 – Two-wire serial ID interface	3
5	MOD-DEF1	Module Definition 1 – Two-wire serial ID interface	3
6	MOD-DEF0	Module Definition 0 – Grounded in module	3
7	Rate Select	Not Connected	
8	LOS	Loss of Signal – High indicates loss of signal	4
9	$V_{EE}R$	Receiver Ground	
10	$V_{EE}R$	Receiver Ground	
11	$V_{EE}R$	Receiver Ground	
12	RD–	Inverse Received Data Out	5
13	RD+	Received Data Out	5
14	$V_{EE}R$	Receiver Ground	
15	$V_{CC}R$	Receiver Power – 3.3 V ± 5%	6
16	$V_{CC}T$	Transmitter Power – 3.3 V ± 5%	6
17	$V_{EE}T$	Transmitter Ground	
18	TD+	Transmitter Data In	7
19	TD–	Inverse Transmitter Data In	7
20	$V_{EE}T$	Transmitter Ground	

Notes:

1. TX Fault is an open collector/drain output, which should be pulled up externally with a 4.7K – 10 KΩ resistor on the host board to a supply < $V_{CC}T$+0.3 V or $V_{CC}R$+0.3 V. When high, this output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to < 0.8 V.
2. TX Disable is an input that is used to shut down the laser output per the state table below. It is pulled up within the module with a 4.7K – 10 KΩ resistor.

Low (0 – 0.8 V):	Transmitter on
Between (0.8 V and 2.0 V):	Undefined
High (2.0 – 3.465 V):	Transmitter Disabled
Open:	Transmitter Disabled

3. Mod-Def 0,1,2. These are the module definition pins. They should be pulled up with a 4.7-10 KΩ resistor on the host board to a supply less than $V_{CC}T$ + 0.3 V or $V_{CC}R$ + 0.3 V.

   Mod-Def 0 is grounded by the Module to indicate that the module is present
   Mod-Def 1 is clock line of two-wire serial interface for optional serial ID
   Mod-Def 2 is data line of two-wire serial interface for optional serial ID

4. LOS (Loss of Signal) is an open collector/drain output that should be pulled up externally with a 4.7K – 10 KΩ resistor on the host board to a supply < $V_{CC}T,R$+0.3 V. When high, this output indicates the received optical power is below the worst case receiver sensitivity. Low indicates normal operation. In the low state, the output will be pulled to < 0.8 V.
5. RD-/+: These are the differential receiver outputs. They are AC coupled 100 Ω differential lines which should be terminated with 100 Ω differential at the user SerDes. The AC coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 400 and 2000 mV differential (200 – 1000 mV single ended) when properly terminated. These levels are compatible with CML and LVPECL voltage swings.
6. $V_{CC}R$ and $V_{CC}T$ are the receiver and transmitter power supplies. They are defined as 3.3 V ± 5% at the SFP connector pin. The associated in-rush power supply current will typically be no more than 30 mA above the steady state supply current after 500 nanoseconds.
7. TD-/+: These are the differential transmitter inputs. They are AC coupled differential lines with 100 Ω differential termination inside the module. The AC coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swings of 400 – 2400 mV (200 – 1200 mV single ended), however the recommended differential voltage swing is found in Table 6. These levels are compatible with CML and LVPECL voltage swings.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Storage Temperature	T_S	–40		100	°C	1
Case Temperature	T_C	–40		85	°C	1, 2
Relative Humidity	RH	5		95	%	1
Module Supply Voltage	V_{CC}T,R	–0.5		3.6	V	1, 2
Data/Control Input Voltage	V_I	–0.5		V_{CC}	V	1
Sense Output Current – LOS,TX Fault	I_D			150	mA	1
MOD DEF2	I_D			5	mA	1

Notes:
1. Absolute Maximum Ratings are those values beyond which damage to the device may occur if these limits are exceeded for other than a short period of time. See Reliability Data Sheets for specific reliability performance.
2. Between Absolute Maximum Ratings and the Recommended Operating Conditions, functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time.

Table 4. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Case Temperature	T_C	0		70	°C	1
Module Supply Voltage	V_{CC}T,R	3.135	3.3	3.465	V	1
Data Rate			1.0625		Gb/s	1

Notes:
1. Recommended operating conditions are those values outside of which functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time. See Reliability Data Sheet for specific reliability performance.

Table 5. Transceiver Electrical Characteristics
(T_C = 0°C to 70°C, V_{CC}T,R = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
AC Electrical Characteristics						
Power Supply Noise Rejection (Peak-to-Peak)	PSNR		100		mV	1
DC Electrical Characteristics						
Module Supply Current	I_{CC}		160	220	mA	
Power Dissipation	P_{DISS}		530	765	mW	
Sense Outputs:						
Transmit Fault (TX_FAULT),	V_{OH}	2.0		V_{CC}T,R + 0.3	V	2
Loss of Signal (LOS), MOD-DEF2	V_{OL}	0.0		0.8	V	2
Control Inputs:						
Transmitter Disable (TX_DISABLE),	V_{IH}	2.0		V_{CC}	V	2
MOD-DEF1,2	V_{IL}	0.0		0.8	V	2

Notes:
1. MSA filter is required on host board 10 Hz to 2 MHz.
2. LVTTL, external 4.7-10 KΩ pull-up resistor required.

Table 6. Transmitter and Receiver Electrical Characteristics
(T_C = 0°C to 70°C, V_{CC}T,R = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Data Input:						
Transmitter Differential Input Voltage (TD +/–)	V_I	400		2000	mV	1
Data Output:						
Receiver Differential Output Voltage (RD +/–)	V_O	400	1500	2000	mV	2
Contributed Total Jitter (Receiver) 1.0625 Gb/s	TJ			205	ps	
				0.218	UI	
Deterministic Jitter (Receiver) 1.0625 Gb/s	DJ			113	ps	
				0.12	UI	
Receive Data Rise & Fall Times (Receiver)	T_{rf}			350	ps	3

Notes:
1. Internally AC coupled and terminated (100 Ohm differential). These levels are compatible with CML and LVPECL voltage swings.
2. Internally AC coupled with an external 100 Ohm differential load termination.
3. 20%-80% Rise & Fall times measured with a 500 MHz signal utilizing a 1010 data pattern.

Table 7. Transmitter Optical Characteristics
(TC = 0°C to 70°C, V_{CC}T,R = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Output Optical Power (Average)	P_{OUT}	–10		0	dBm	50/125 µm NA = 0.2 Note 1
	P_{OUT}	–10		0	dBm	62.5/125 µm NA = 0.275 Note 1
Optical Extinction Ratio	ER	9			dB	2
Optical Modulation Amplitude (Peak-to-Peak) 1.0625 Gb/s	OMA	156			µW	FC-PI Std
Center Wavelength	λ_C	830		860	nm	FC-PI Std
Spectal Width – rms	σ			1.0	nm	FC-PI Std
Optical Rise /Fall Time	$T_{rise/fall}$			300	ps	20%–80%, FC-PI Std
RIN_{12}(OMA), maximum	RIN			–116	dB/Hz	FC-PI Std
Contributed Total Jitter (Transmitter) 1.0625 Gb/s	TJ			0.267	UI	
				252	ps	
Deterministic Jitter (Receiver) 1.0625 Gb/s	DJ			85	ps	
				0.09	UI	
P_{OUT} TX_DISABLE Asserted	P_{OFF}			–35	dBm	

Notes:
1. Max P_{OUT} is the lesser of 0 dBm or maximum allowable per Eye Safety Standard.
2. Required for compliance to FC-PH-2.

Table 8. Receiver Optical Characteristics
(TC = 0°C to 70°C, $V_{CC}T,R$ = 3.3 V ± 5%)

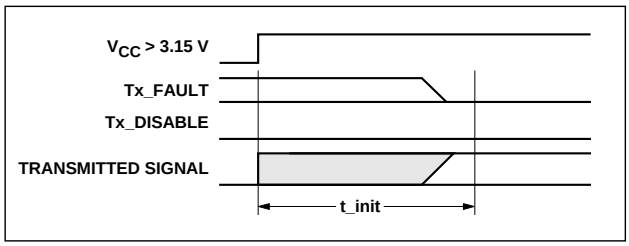
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Optical Power	PIN	–17		0	dBm	FC-PI Std, 1
Min Optical Modulation Amplitude (Peak-to-Peak) 1.0625 Gb/s	OMA	31			µW	FC-PI Std, 2
Stressed Receiver Sensitivity (OMA) 1.0625 Gb/s		55			µW	50 µm fiber, FC-PI Std
		67			µW	62.5 µm fiber, FC-PI Std
Return Loss		12			dB	FC-PI Std
Loss of Signal – Assert	P_A	–31		–17.5	dBm	4
Loss of Signal – De-assert	P_D			–17.0	dBm	4
Loss of Signal Hysteresis	$P_D – P_A$	0.5		5	dB	

Notes:
1. Required for compliance to FC-PH-2.
2. An OMA of 31 is approximately equal to an average power of –17 dBm assuming an Extinction Ratio of 9 dB. Sensitivity measurements are made at eye center with BER = 10E–12.
3. 1.0625 Gb/s stressed receiver vertical eye closure penalty (ISI) minimum is 0.96 dB for 50 µm fiber and 2.18 dB for 62.5 µm fiber. Stressed receiver DCD component minimum (at TX) is 80 ps.
4. These average power values are specified with an Extinction Ratio of 9 dB. The Loss of Signal circuitry responds to OMA (peak-to-peak) power, not to average power.

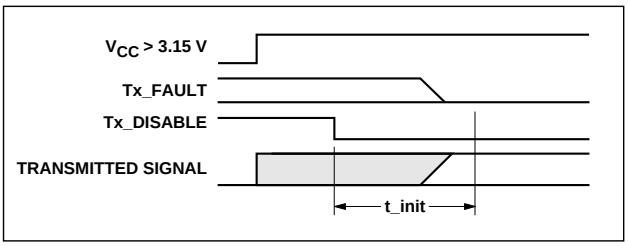
Table 9. Transceiver Timing Characteristics
(TC = 0°C to 70°C, $V_{CC}T,R$ = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
TX Disable Assert Time	t_off			10	µs	1
TX Disable Negate Time	t_on			1	ms	2
Time to Initialize, including Reset of TX_FAULT	t_init			300	ms	3
TX Fault Assert Time	t_fault			100	µs	4
TX Disable to Reset	t_reset	10			µs	5
LOS Assert Time	t_loss_on			100	µs	6
LOS De-assert Time	t_loss_off			100	µs	7
Serial ID Clock Rate	F_serial_clock			100	kHz	

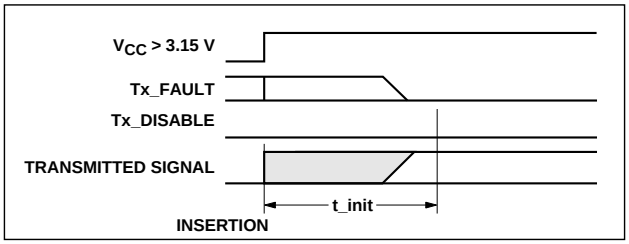
Notes:
1. Time from rising edge of TX Disable to when the optical output falls below 10% of nominal.
2. Time from falling edge of TX Disable to when the modulated optical output rises above 90% of nominal.
3. From power on or negation of TX Fault using TX Disable.
4. Time from fault to TX fault on.
5. Time TX Disable must be held high to reset TX_FAULT.
6. Time from LOS state to RX LOS assert per Figure 6.
7. Time from non-LOS state to RX LOS de-assert per Figure 6.



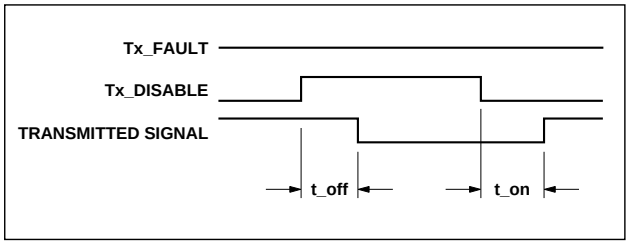
t-init: TX DISABLE NEGATED



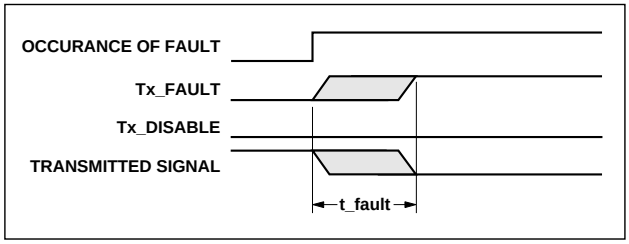
t-init: TX DISABLE ASSERTED



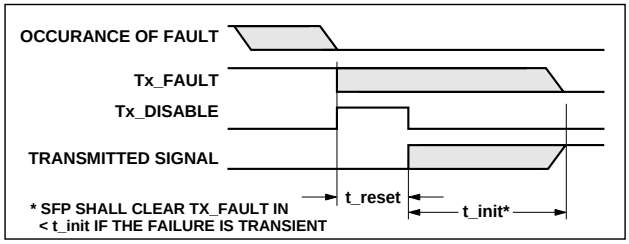
t-init: TX DISABLE NEGATED, MODULE HOT PLUGGED



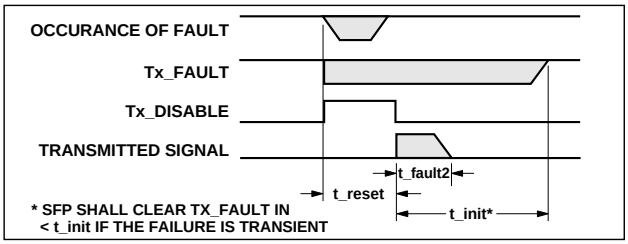
t-off & t-on: TX DISABLE ASSERTED THEN NEGATED



t-fault: TX FAULT ASSERTED, TX SIGNAL NOT RECOVERED

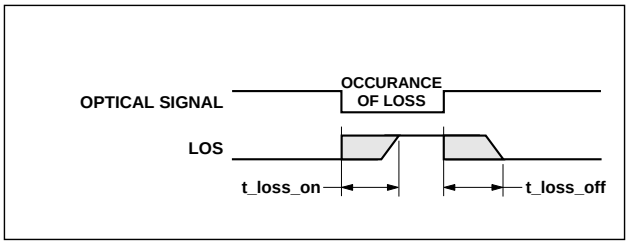


t-reset: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL RECOVERED



t-fault2: TX DISABLE ASSERTED THEN NEGATED,
TX SIGNAL NOT RECOVERED

NOTE: t_fault2 typical 1.7 to 2.0 ms.



t-loss-on & t-loss-off

Figure 6. Transceiver timing diagrams (module installed except where noted).

Table 10. EEPROM Serial ID Memory Contents

Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII
0	03		40	48	H	68	Note 1		96		
1	04		41	46	F	69	Note 1		97		
2	07		42	42	B	70	Note 1		98		
3	00		43	52	R	71	Note 1		99		
4	00		44	2D	–	72	Note 1		100		
5	00		45	35	5	73	Note 1		101		
6	00		46	37	7	74	Note 1		102		
7	20		47	33	3	75	Note 1		103		
8	40		48	30	0	76	Note 1		104		
9	0C		49	4C	L	77	Note 1		105		
10	01		50	20		78	Note 1		106		
11	01		51	20		79	Note 1		107		
12	0B		52	20		80	Note 1		108		
13	00		53	20		81	Note 1		109		
14	00		54	20		82	Note 1		110		
15	00		55	20		83	Note 1		111		
16	32		56	20		84	Note 2		112		
17	1E		57	20		85	Note 2		113		
18	00		58	20		86	Note 2		114		
19	00		59	20		87	Note 2		115		
20	41	A	60	00		88	Note 2		116		
21	47	G	61	00		89	Note 2		117		
22	49	I	62	00		90	20		118		
23	4C	L	63	Note 3		91	20		119		
24	45	E	64	00		92	00		120		
25	4E	N	65	1A		93	00		121		
26	54	T	66	00		94	00		122		
27	20		67	00		95	Note 3		123		
28	20								124		
29	20								125		
30	20								126		
31	20								127		
32	20										
33	20										
34	20										
35	20										
36	00										
37	00										
38	30										
39	D3										

Notes:
1. Address 61–83 specify a unique identifier.
2. Address 84–91 specify the date code.
3. Addresses 63 and 95 are check sums. Address 63 is the check sum for bytes 0–62 and address 95 is the check sum for bytes 64–94.

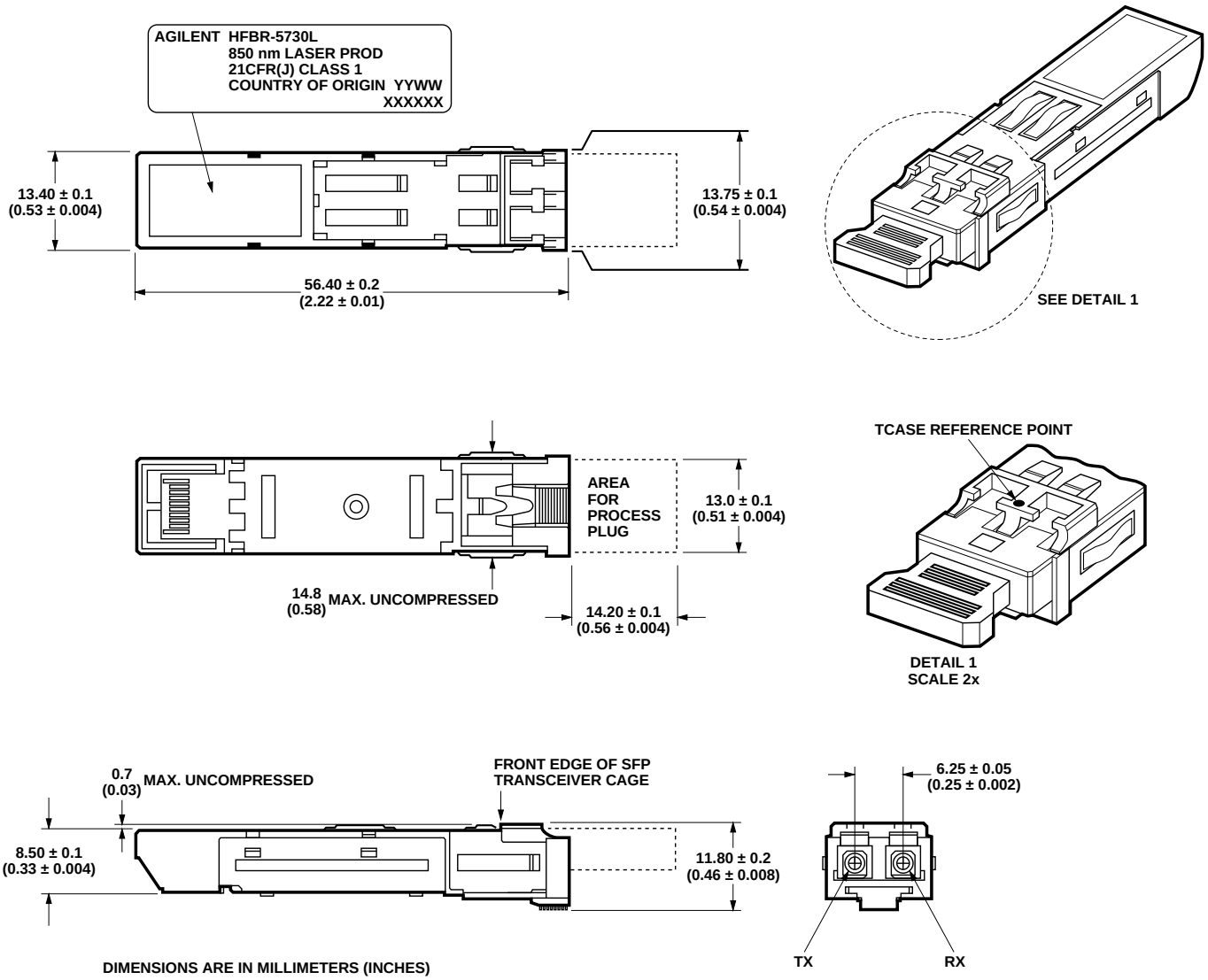


Figure 7a. Module drawing.

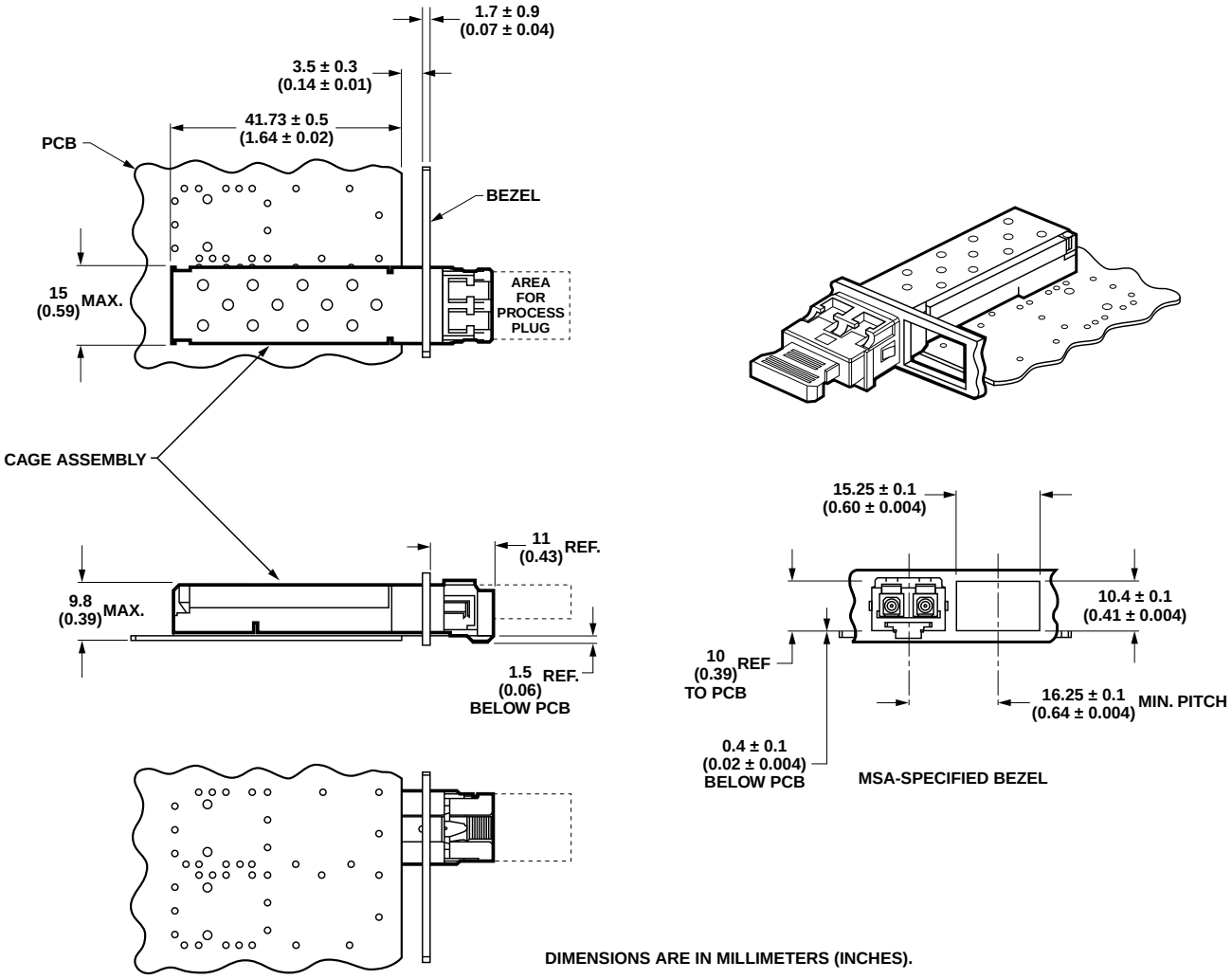
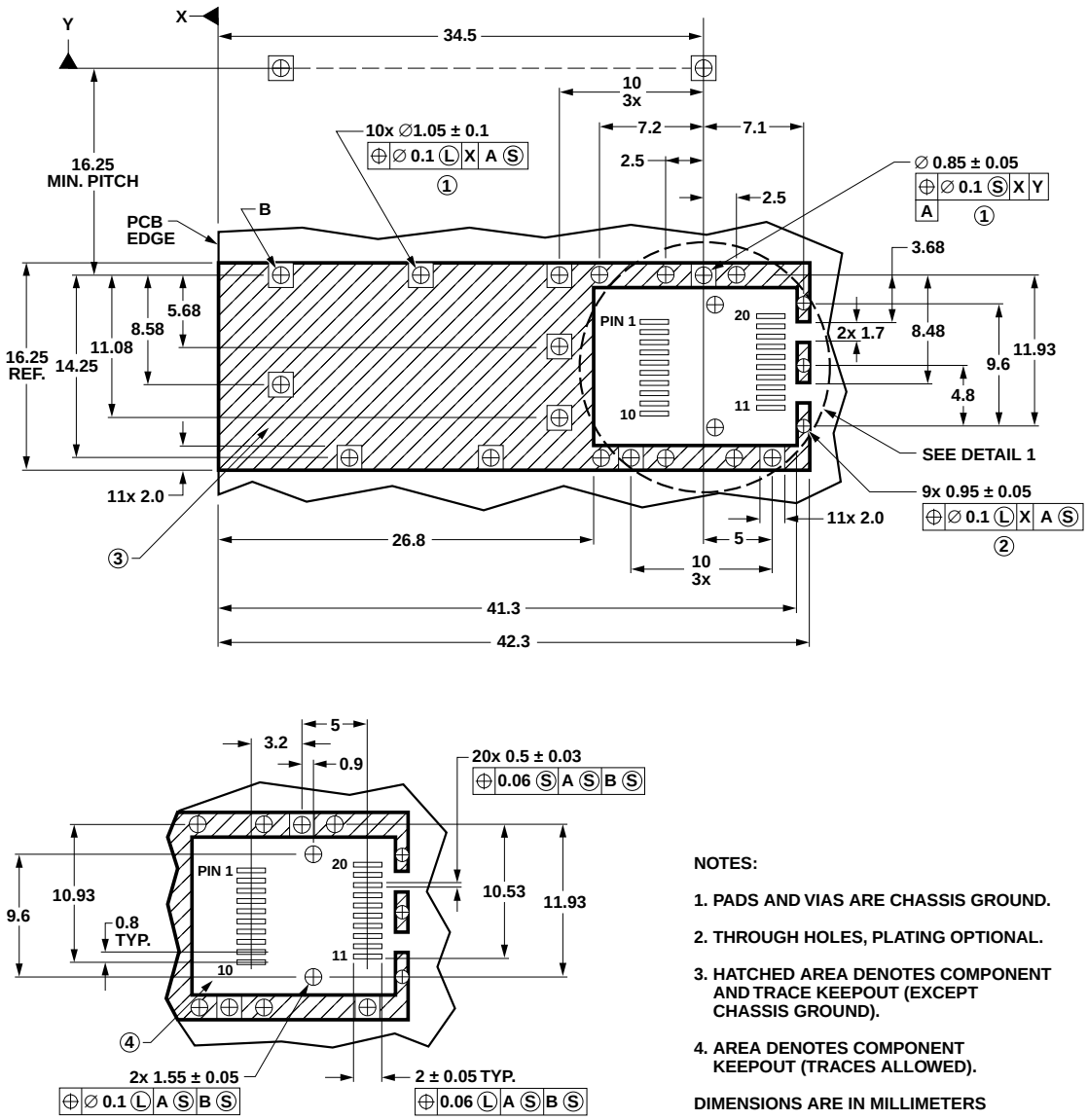


Figure 7b. Assembly drawing.



DETAIL 1

NOTES:

1. PADS AND VIAS ARE CHASSIS GROUND.
2. THROUGH HOLES, PLATING OPTIONAL.
3. HATCHED AREA DENOTES COMPONENT AND TRACE KEEPOUT (EXCEPT CHASSIS GROUND).
4. AREA DENOTES COMPONENT KEEPOUT (TRACES ALLOWED).

DIMENSIONS ARE IN MILLIMETERS

Figure 7c. SFP host board mechanical layout.

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Data subject to change.

Obsoletes 5988-3384EN

July 15, 2002

5988-7282EN

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