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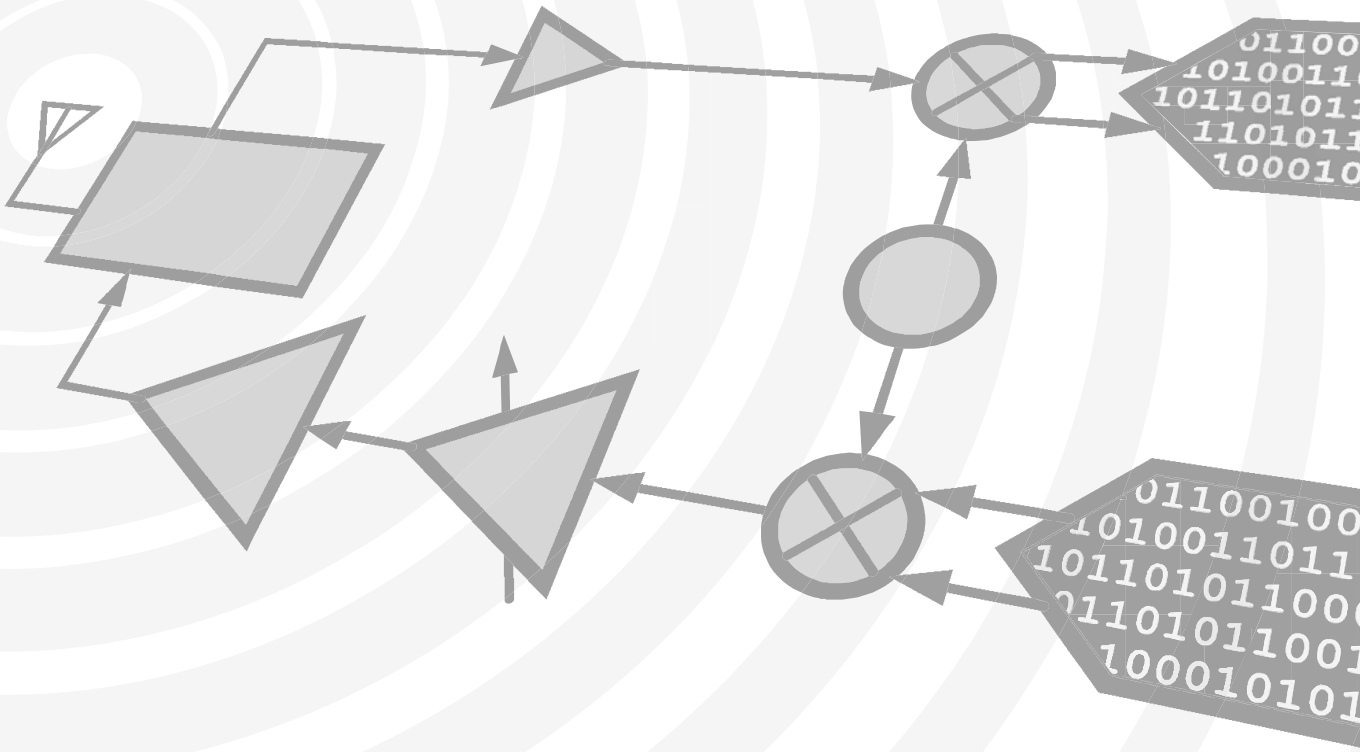

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v03.0914

HMC842LC4B

45 Gbps, FANOUT BUFFER w/ PROGRAMMABLE OUTPUT VOLTAGE

Typical Applications

The HMC842LC4B is ideal for:

- OC-768 and SDH STM-256 Equipment
- RF ATE Applications
- Short, intermediate, & Long Haul Fiber Optic Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 45 Gbps
- Clock Buffering up to 28 GHz

Features

Supports Clock Frequencies up to 28 GHz

Independent Programmable Output Swing for Each Channel: 400 - 1200 mVp-p Diff.

Supports Single-Ended or Differential Operation

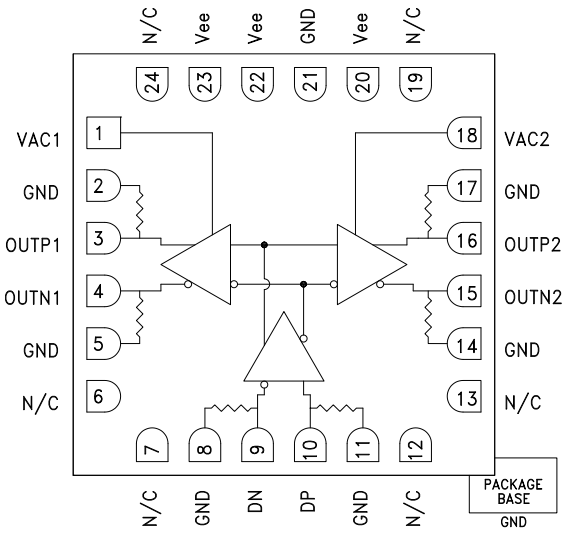
Power Consumption: 465 mW

Less than 500 fs Additive RMS Jitter

Fast Rise and Fall Times: <12ps

24 Lead 4x4mm SMT Package: $16mm^2$

Functional Diagram



General Description

The HMC842LC4B is a 1:2 Fanout Buffer designed to support data transmission rates up to 45 Gbps. The device can also operate with clock signals up to 28 GHz. During normal operation, input data (or clock) is transferred to both output channels. Differential input and output signals of the HMC842LC4B are terminated with 50 Ohms to ground on-chip, and may be either AC or DC coupled. The Outputs can be connected directly to a 50 Ohms-to-ground terminated system, while DC blocking capacitors should be used if the terminating system is 50 Ohms to a non-ground DC voltage.

The HMC842LC4B also features two separate output level control pins, VAC1 and VAC2 which provide loss compensation and signal level optimization for each output channel independently. The HMC842LC4B operates from a single -3.3V DC supply and is available in a ceramic RoHS compliant 4 x 4 mm SMT package.

Electrical Specifications, T_A = +25°C, Vee = -3.3V

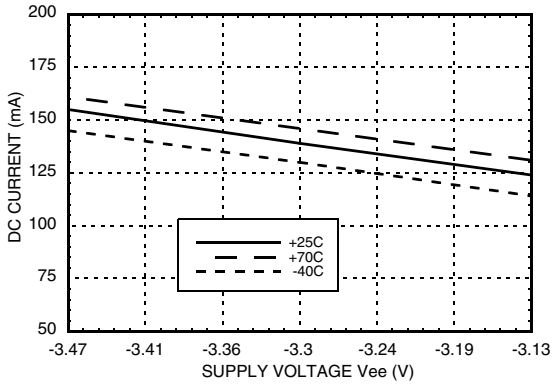
Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage	±5 % Tolerance	-3.47	-3.3	-3.13	V
Power Supply Current	VAC1 = VAC2 = -0.3V (Vout = 930 mVp-p diff @ 40 Gbps)	120	140	160	mA
Output Amplitude Control Voltage [1] (VAC1, VAC2)		-1.4	-0.3	0	V
Maximum Data Rate		45			Gbps
Maximum Clock Rate		28	32		GHz
Input Amplitude	Single-ended, peak-to-peak	50		1000	mVp-p
	Differential, peak-to-peak	100		2000	
Input High Voltage		-0.5		0.5	V
Input Low Voltage		-1		0	V

Electrical Specifications, (continued)

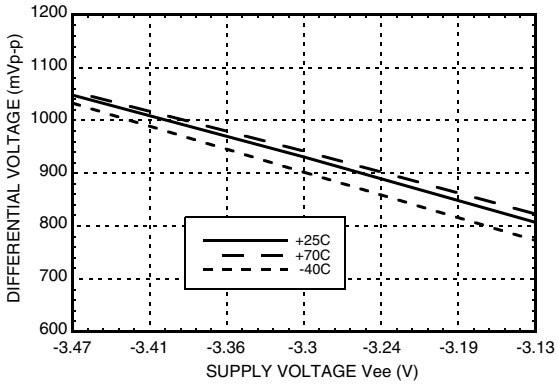
Parameter	Conditions	Min.	Typ.	Max	Units
Output Amplitude	Differential, peak-to-peak @ 40 Gbps	400		1200	mVp-p
Output High Voltage		VAC = -0.3	-10		mV
Output Low Voltage		VAC = -0.3	-550		mV
Input Return Loss	frequency < 32 GHz		10		dB
Output Return Loss	frequency < 32 GHz		7		dB
Deterministic Jitter, Jd [2]			3		ps, pp
Additive Random Jitter Jr	@ 28 GHz Clock Input			0.3	ps rms
	@ 32 GHz Clock Input			0.6	ps rms
Rise Time, tr [2]			11		ps
Fall Time, tf [2]			11		ps
Propagation Delay, td			10		ps
OUT1 to OUT2 Data Skew, t_{skew} [2]			2		ps

[1] VAC1=VC2 and VAC2=VC1 on evaluation board
[2] Data Input: 40 Gbps PRBS 2^{23}-1 pattern, 150 mVp-p single-ended

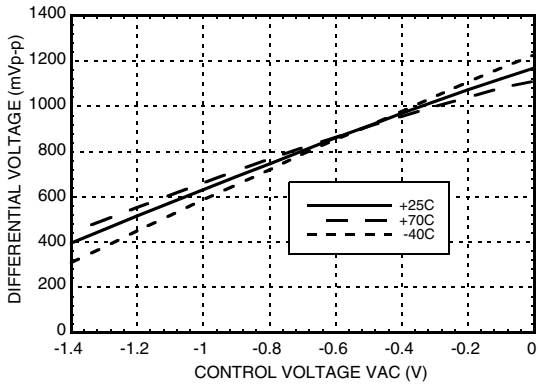
DC Current vs. Supply Voltage [1] [2]



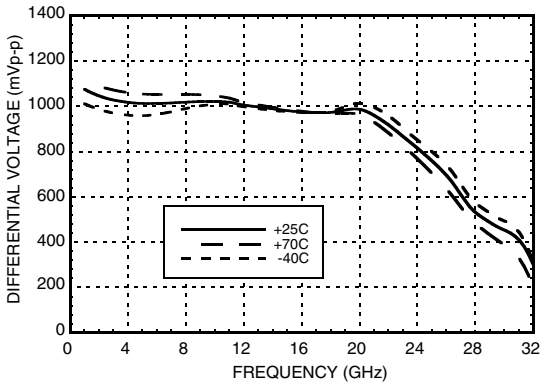
Differential Output Swing vs. Supply Voltage [1] [2]



Differential Output Swing vs. VAC [3]



Differential Output Swing vs. Frequency [1]

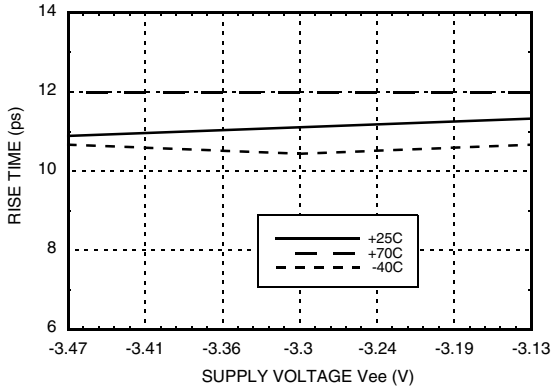


[1] VAC = -0.3V [2] Input data rate: 40 Gbps PRBS 2^{23}-1 [3] Frequency = 20 GHz

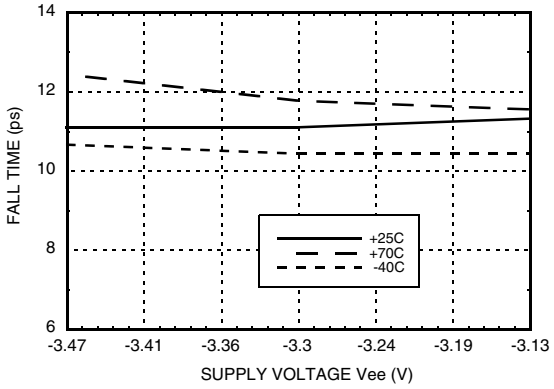
HMC842LC4B

45 Gbps, FANOUT BUFFER w/ PROGRAMMABLE OUTPUT VOLTAGE

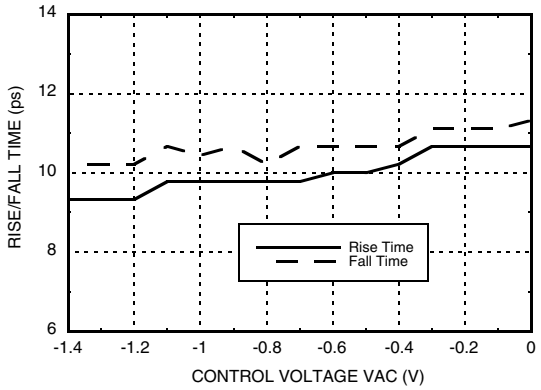
Rise Time vs. Supply Voltage [1][2][3]



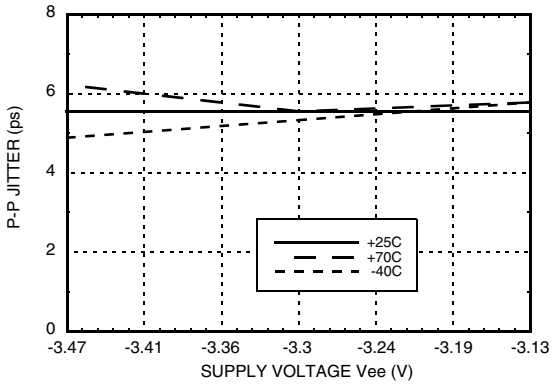
Fall Time vs. Supply Voltage [1][2][3]



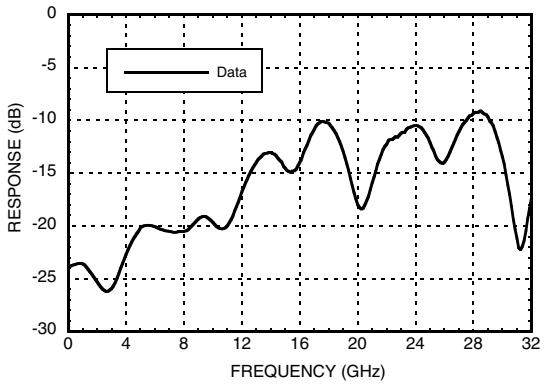
Rise / Fall Time vs. VAC [1][2][3]



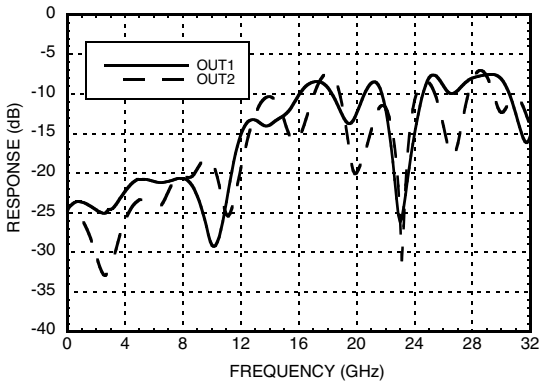
Peak-to-Peak Jitter vs. Supply Voltage [1][2][3][4]



Input Return Loss vs. Frequency [1][5]

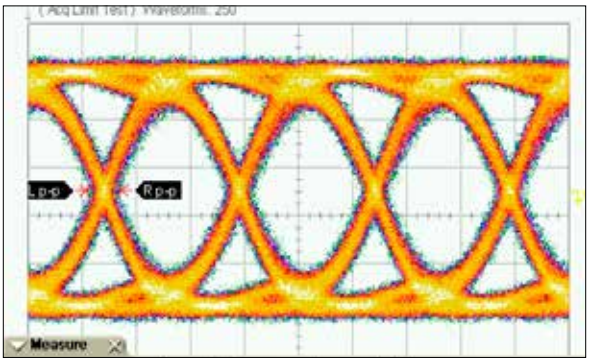


Output Return Loss vs. Frequency [1][5]



[1] VAC = -0.3V [2] Input data rate: 40 Gbps PRBS 2^{23}-1 [3] Data was taken at single ended output
[4] Source jitter was not deembeded [5] Device measured on evaluation board with single-ended time domain gating.

40 Gbps Differential Output Eye Diagram

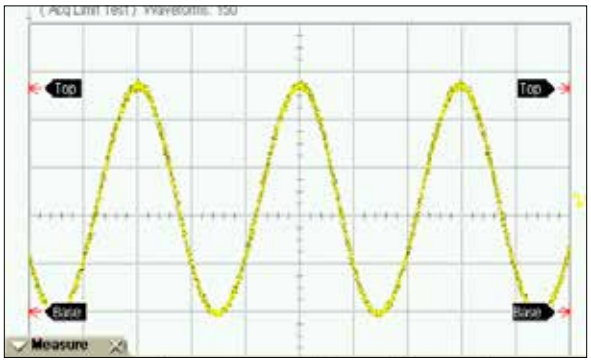


Measurements				
	Current	Min	Max	Total Meas.
Eye Amp	921 mV	920 mV	922 mV	75
Rise Time	11.11 ps	10.89 ps	11.11 ps	75
Fall Time	11.11 ps	10.44 ps	11.11 ps	75
p-p Jitter	5.778 ps	5.333 ps	5.778 ps	75

Time Scale: 10 ps/div
Amplitude Scale: 210 mV/div

Test Conditions:
Vee = -3.3V, VAC = -0.3V
Input Data: Single ended 150 mVp-p 40 Gbps NRZ PRBS 2^{23}-1 pattern

28 GHz Differential Output Eye Diagram

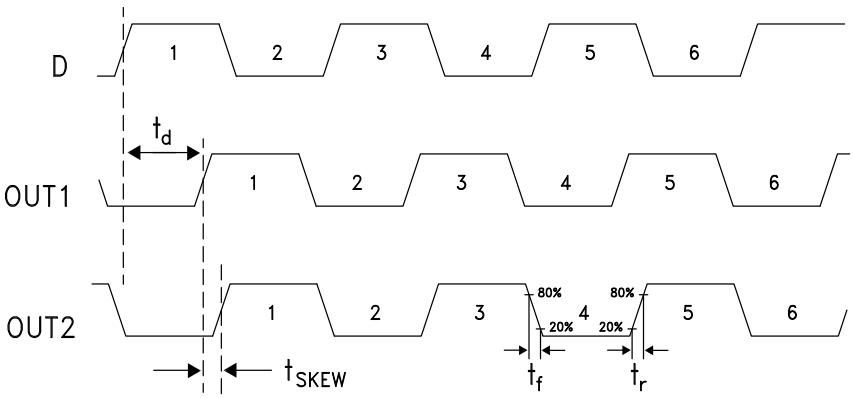


Measurements				
	Current	Mean	Min	Max
V Amp	558.99 mV	556.8 mV	543.46 mV	577.62 mV
Rise Time	6.86 ps	6.816 ps	6.28 ps	7.43 ps
Fall Time	6.91 ps	6.473 ps	5.84 ps	7.01 ps

Time Scale: 12 ps/div
Amplitude Scale: 120 mV/div

Test Conditions:
Vee = -3.3V, VAC = -0.3V
Input Data: Single ended 300 mVp-p 28 GHz clock signal

Timing Diagram



Input	Outputs	
D	OUT1	OUT2
L	L	L
H	H	H
Notes: D = DP - DN OUT1 = OUTP1 - OUTN1 OUT2 = OUTP2 - OUTN2	H - Logic High L - Logic Low	

HMC842LC4B

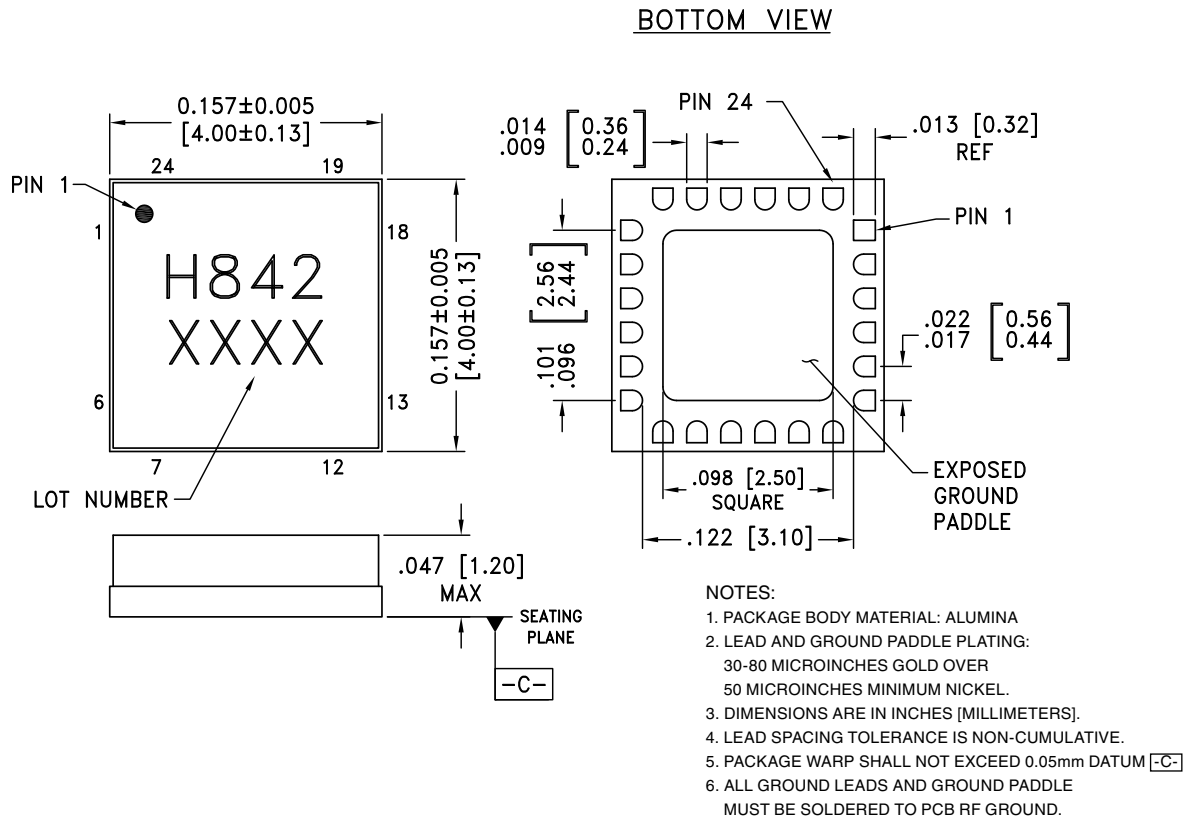
45 Gbps, FANOUT BUFFER w/ PROGRAMMABLE OUTPUT VOLTAGE

Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.7V to +0.5V
Input Voltage	-1.3V to +0.5V
Channel Temperature	125°C
Continuous Pdiss (T = 85°C) (derate 18.48 mW/°C above 85°C)	0.74 W
Thermal Resistance (channel to ground paddle)	54.11 °C/W
Storage Temperature	-65°C to +125°C
Operating Temperature	-40°C to +70°C
Output Amplitude Control Voltage (VAC)	-2.3V to +0.5V

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



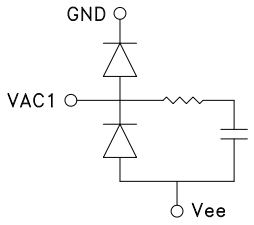
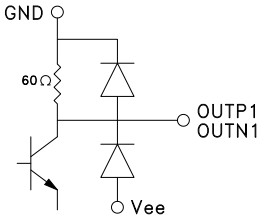
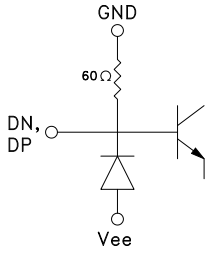
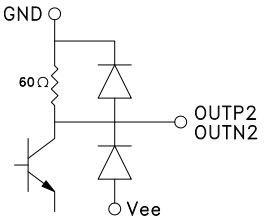
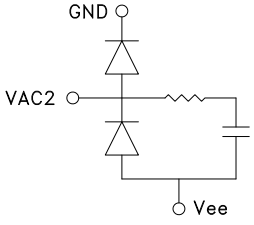
NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER
   50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Package Information

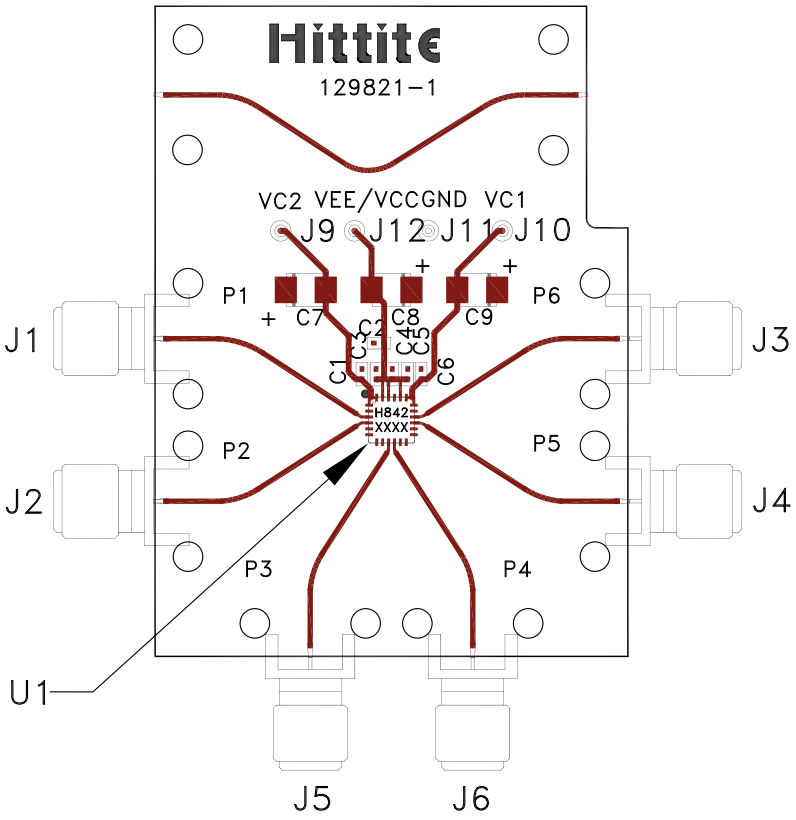
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC842LC4B	Alumina, White	Gold over Nickel	MSL3 [1]	H842 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	VAC1	Output Amplitude Control Voltage for OUT1 Note: VAC1=VC2 on evaluation board	
2, 5, 8, 11, 14, 17, 21 Package Bottom	GND	Signal and supply grounds	
3, 4	OUTP1, OUTN1	Differential (OUTP1-OUTN1) or single ended (OUTP1) outputs	
6, 7, 12, 13, 19, 24	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
9, 10	DN, DP	Differential (DP-DN) or single ended (DP) inputs	
15, 16	OUTN2, OUTP2	Differential (OUTP2-OUTN2) or single ended (OUTP2) outputs	
18	VAC2	Output Amplitude Control Voltage for OUT2 Note: VAC2=VC1 on evaluation board	
20, 22, 23	Vee	Power Supply (-3.3V)	

Evaluation PCB



Note: VC1 on evaluation board is VAC2 and VC2 on evaluation board is VAC1

Item	Description
J1	OUTP1
J2	OUTN1
J3	OUTP2
J4	OUTN2
J5	DN
J6	DP
J9	VAC1
J10	VAC2
J11	GND
J12	Vee

List of Materials for Evaluation PCB 129151 [1]

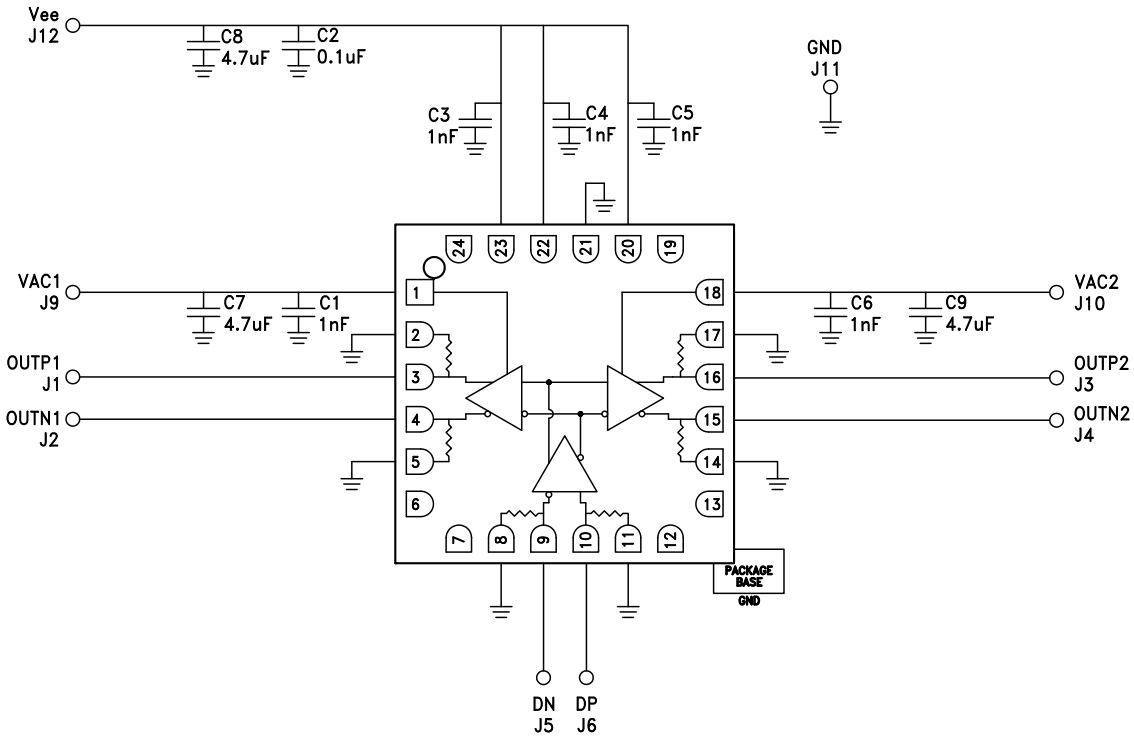
Item	Description
J1 - J6	K Connector
J9 - J12	DC Pin
C1, C3 - C6	1000 pF Capacitor, 0402 Pkg.
C2	0.1 µF Capacitor, 0402 Pkg.
C7 - C9	4.7 µF Capacitor, Tantalum
U1	HMC842LC4B 1:2 Fanout Buffer
PCB [2]	129821 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed metal package base must be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit



Note: VAC1(J9)=VC2 and VAC2(J10)=VC1 on evaluation board.

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