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### 3.3V SDRAM Buffer for Mobile PCs with 4 SO-DIMMs

## Features

- One input to 10 output buffer/driver
- Supports up to four SDRAM SO-DIMMs
- Two additional outputs for feedback
- Serial interface for output control
- Low skew outputs
- Up to 133 MHz operation
- Multiple $V_{D D}$ and $V_{S S}$ pins for noise reduction
- Dedicated OE pin for testing
- Space-saving 28 Pin SSOP package
- 3.3V operation


## Functional Description

The ASM2I2310ANZ is a 3.3 V buffer designed to distribute high-speed clocks in mobile PC applications. The part has 10 outputs, 8 of which can be used to drive up to four SDRAM SO-DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3 V and outputs can run up to 133 MHz , thus making it compatible with Pentium II ${ }^{\text {®i }}$ processors.

The ASM2I2310ANZ also includes a serial interface (IIC), which can enable or disable each output clock. The IIC is Slave Receiver only and is Standard mode compliant. IIC Master can write into the IIC registers but cannot read back. The first two bytes after address should be ignored by IIC Block and data is valid after these two bytes as given in IIC Byte Flow Table. On power-up, all output clocks are enabled. A separate Output Enable pin facilitates testing on ATE.

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## Pin Configuration

## 28 Pin SSOP Package-- Top View



## Pin Description

| Pins | Name | Type | Description |
| :---: | :---: | :---: | :---: |
| 1, 5, 10, 19, 24, 28 | $\mathrm{V}_{\mathrm{DD}}$ | P | 3.3V Digital voltage supply |
| 4, 8, 12, 17, 21, 25 | $\mathrm{V}_{\text {ss }}$ | P | Ground |
| 13 | $V_{\text {DDIIC }}$ | P | 3.3V Serial interface voltage supply |
| 16 | $V_{\text {ssuc }}$ | P | Ground for serial interface |
| 9 | BUF_IN | 1 | Input clock, 5V tolerant |
| 20 | OE | 1 | Output Enable, three-states outputs when LOW. Internal pull-up to $V_{D D}$ |
| 14 | SDATA | 1/0 | Bi-directional Serial data pin. Internal pull-up to $\mathrm{V}_{\text {DD }} .5 \mathrm{~V}$ tolerant |
| 15 | SCLK | I | Serial clock input. Internal pull-up to $\mathrm{V}_{\text {DD }} .5 \mathrm{~V}$ tolerant |
| 2, 3, 6, 7 | SDRAM [0-3] | 0 | SDRAM byte 0 Clock Outputs |
| 22, 23, 26,27 | SDRAM [4-7] | $\bigcirc$ | SDRAM byte 1 Clock Outputs |
| 11, 18 | SDRAM [8-9] | 0 | SDRAM byte 2 Clock Outputs |

## Device Functionality

| OE | SDRAM [0-17] |
| :---: | :---: |
| 0 | High-Z |
| 1 | $1 \times$ BUF_IN |

## Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte N-Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits can be programmed to either " 0 " or " 1 ".
- Serial interface address for the ASM2I2310ANZ is:

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | --- |

Byte 0: SDRAM Active/Inactive Register ${ }^{1}$ ( $1=$ Enable, 0 = Disable), Default = Enable

| Bit | Pin \# | Description |
| :---: | :---: | :--- |
| Bit 7 | -- | Unused |
| Bit 6 | -- | Unused |
| Bit 5 | -- | Unused |
| Bit 4 | -- | Unused |
| Bit 3 | 7 | SDRAM3 (Active/Inactive) |
| Bit 2 | 6 | SDRAM2 (Active/Inactive) |
| Bit 1 | 3 | SDRAM1 (Active/Inactive) |
| Bit 0 | 2 | SDRAM0 (Active/Inactive) |

Note 1: When the value of bit in these bytes is high, the output is enabled. When the value of the bit is low, the output is forced to low state. The default value of all the bits is high after chip is powered up.

IIC Byte Flow

| Byte | Description |
| :---: | :---: |
| 1 | IIC Address |
| 2 | Command (dummy value, ignored) |
| 3 | Byte Count (dummy value, ignored) |
| 4 | IIC Data Byte 0 |
| 5 | IIC Data Byte 1 |
| 6 | IIC Data Byte 2 |

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## Absolute Maximum Ratings

| Symbol | Parameter | Rating | Unit |
| :---: | :--- | :---: | :---: |
| $V_{D D}$ | Supply Voltage to Ground Potential | -0.5 V to +7.0 | V |
| $\mathrm{~V}_{I N}$ | DC Input Voltage (Except BUF_IN) | -0.5 V to $\mathrm{V}_{\mathrm{DD}}+0.5$ | V |
| $\mathrm{~V}_{I N B}$ | DC Input Voltage (BUF_IN) | -0.5 V to +7.0 | V |
| $\mathrm{~T}_{S T G}$ | Storage Temperature | $-65^{\circ} \mathrm{C}$ to +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{J}$ | Junction Temperature | 150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{DV}}$ | Static Discharge Voltage <br> (As per JEDEC STD 22-A114-B) | 2000 | V |

## Operating Conditions

| Parameter | Description | Min | Max | Unit |
| :---: | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{DD}}$ | Supply Voltage | 3.135 | 3.465 | V |
| $\mathrm{~T}_{\mathrm{A}}$ | Operating Temperature (Ambient Temperature) | 0 | 70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{C}_{\mathrm{L}}$ | Load Capacitance | 20 | 30 | pF |
| $\mathrm{C}_{\mathrm{IN}}$ | Input Capacitance |  | 7 | pF |
| $\mathrm{t}_{\mathrm{PU}}$ | Power-up time for all $\mathrm{V}_{\mathrm{DD}}$ 's to reach minimum specified voltage <br> (power ramps must be monotonic) | 0.05 | 50 | ms |

Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VIL | Input LOW Voltage | Except serial interface pins |  |  | 0.8 | V |
| $\mathrm{V}_{\text {ILIIC }}$ | Input LOW Voltage | For serial interface pins only |  |  | 0.7 | V |
| $\mathrm{V}_{\text {IH }}$ | Input HIGH Voltage |  | 2.0 |  |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Output LOW Voltage ${ }^{1}$ | $\mathrm{I}_{\mathrm{OL}}=25 \mathrm{~mA}$ |  |  | 0.4 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | Output HIGH Voltage ${ }^{1}$ | $\mathrm{I}_{\mathrm{OH}}=-36 \mathrm{~mA}$ | 2.4 |  |  | V |
| Icc | Quiescent Supply Current | $\begin{aligned} & V_{D D}=3.465 \mathrm{~V}, \mathrm{~V}_{\mathrm{i}}=\mathrm{V}_{\mathrm{DD}} \text { or } \mathrm{GND} \\ & \mathrm{l}_{\mathrm{O}}=0 \end{aligned}$ |  | 50 | 100 | $\mu \mathrm{A}$ |
| loz | High Impedance Output Current | $V_{D D}=3.465 \mathrm{~V}, \mathrm{~V}_{\mathrm{i}}=\mathrm{V}_{\mathrm{DD}} \text { or } \mathrm{GND}$ |  |  | $\pm 10$ | $\mu \mathrm{A}$ |
| loff | OffState Current (for SCL ,SDATA) | $\mathrm{V}_{\mathrm{DD}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{i}}=0 \mathrm{~V}$ or 5.5 V |  |  | 50 | $\mu \mathrm{A}$ |
| $\Delta l_{\text {cc }}$ | Change in Supply Current | $V_{D D}=3.135 \mathrm{~V} \text { to } 3.465 \mathrm{~V}$ <br> One Input at $\mathrm{V}_{\mathrm{DD}}-0.6$, All other Inputs at $\mathrm{V}_{\mathrm{DD}}$ or GND |  |  | 500 | $\mu \mathrm{A}$ |
| I | Input Leakage | $V_{D D}=3.465 \mathrm{~V}$ or $G N D$ (Applicable to all Input Pins) | -5 |  | +5 | $\mu \mathrm{A}$ |
| IDD | Supply Current ${ }^{1}$ | Unloaded outputs, 133 MHz |  |  | 266 | mA |
| $\mathrm{I}_{\mathrm{DD}}$ | Supply Current ${ }^{1}$ | Loaded outputs, 30pF, 133MHz |  |  | 360 | mA |
| IDD | Supply Current ${ }^{1}$ | Unloaded outputs, 100 MHz |  |  | 200 | mA |
| $\mathrm{I}_{\mathrm{DD}}$ | Supply Current ${ }^{1}$ | Loaded outputs, $30 \mathrm{pF}, 100 \mathrm{MHz}$ |  |  | 290 | mA |
| IDD | Supply Current ${ }^{1}$ | Unloaded outputs, 66.67 MHz |  |  | 150 | mA |
| IDD | Supply Current ${ }^{1}$ | Loaded outputs, 30pF , 66.67 MHz |  |  | 185 | mA |
| $\mathrm{I}_{\text {DDS }}$ | Supply Current | BUF_IN= $\mathrm{V}_{\mathrm{DD}}$ or $\mathrm{V}_{\mathrm{SS}}$, all other inputs at $V_{D D}$ |  |  | 500 | $\mu \mathrm{A}$ |

Note: 1. Parameter is guaranteed by design and characterization. Not $100 \%$ tested in production.
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Switching Characteristics ${ }^{1}$

| Parameter | Name | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\text {max }}$ | Maximum Operating Frequency |  |  |  | 133 | MHz |
| $t_{D}$ | Duty $\mathrm{Cycle}^{2,3}=\mathrm{t}_{2} \div \mathrm{t}_{1}$ | Measured at 1.5 V | 45.0 | 50.0 | 55.0 | \% |
| $t_{3}$ | Rising Edge Rate ${ }^{3}$ | Measured between 0.4 V and 2.4 V | 1 | 2 | 4 | V/nS |
| $\mathrm{t}_{4}$ | Falling Edge Rate ${ }^{3}$ | Measured between 2.4 V and $0.4 \mathrm{~V}$ | 1 | 2 | 4 | V/nS |
| $t_{5}$ | Output to Output Skew ${ }^{3}$ | All outputs equally loaded |  | 150 | 225 | pS |
| $\mathrm{t}_{6}$ | SDRAM Buffer LH Prop. Delay ${ }^{3}$ | Input edge greater than $1 \mathrm{~V} / \mathrm{nS}$ | 1 | 2.7 | 3.5 | nS |
| $\mathrm{t}_{7}$ | SDRAM Buffer HL Prop. Delay ${ }^{3}$ | Input edge greater than $1 \mathrm{~V} / \mathrm{nS}$ | 1 | 2.7 | 3.5 | nS |
| $\mathrm{t}_{\text {PLZ }}$ t ${ }_{\text {PHZ }}$ | SDRAM Buffer Enable Delay ${ }^{3}$ | Input edge greater than $1 \mathrm{~V} / \mathrm{nS}$ | 1 | 3 | 5 | nS |
| $\mathrm{t}_{\text {PzL, }} \mathrm{t}_{\text {PzH }}$ | SDRAM Buffer Disable Delay ${ }^{3}$ | Input edge greater than $1 \mathrm{~V} / \mathrm{nS}$ | 1 | 3 | 5 | nS |
| $\mathrm{tr}_{r}$ | Rise Time for SDATA (Refer Test Circuit for IIC) Refer figure no. 3 | $\mathrm{C}_{\mathrm{L}}=10 \mathrm{pF}$ | 6 |  |  | nS |
|  |  | $\mathrm{C}_{\mathrm{L}}=400 \mathrm{pF}$ |  |  | 250 |  |
| $\mathrm{t}_{\mathrm{f}}$ | Fall Time for SDATA (Refer Test Circuit for IIC) Refer figure no. 3 | $\mathrm{C}_{\mathrm{L}}=10 \mathrm{pF}$ | 20 |  |  | nS |
|  |  | $\mathrm{C}_{\mathrm{L}}=400 \mathrm{pF}$ |  |  | 250 |  |

Note: 1 .All parameters specified with loaded outputs.
2. Duty cycle of input clock is $50 \%$. Rising and falling edge rate is greater than $1 \mathrm{~V} / \mathrm{nS}$
3. Parameter is guaranteed by design and characterization. Not $100 \%$ tested in production.

Test Circuit for SDRAM Enable and Disable Times


Figure 1. Load circuit for Switching times
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SDRAM Enable and Disable Times
$\mathrm{V}_{\mathrm{M}}=1.5 \mathrm{~V}$
$V_{\mathrm{X}}=\mathrm{V}_{\mathrm{oL}}+0.3 \mathrm{~V}$
$V_{Y}=V_{\text {он }}-0.3 \mathrm{~V}$
$\mathrm{V}_{\text {он }}$ and $\mathrm{V}_{\text {ol are }}$ the typical Output Voltage drop that occur with the output load


Figure 2. 3-State Enable and Disable times

## Test Circuit for IIC Rise and Fall Times



Figure 3. Test Circuit for IIC
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## Switching Waveforms

## Duty Cycle Timing



## All Outputs Rise/Fall Time



## Output - Output Skew



SDRAM Buffer LH and HL Propagation Delay

InPuT


Test Circuits

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Application Information
Clock traces must be terminated with either series or parallel termination, as is normally done.


## Summary

- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of $0.1 \mu \mathrm{~F}$. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where Rtrace is the loaded characteristic impedance of the trace, Rout is the output impedance of the buffer (typically $25 \Omega$ ), and Rseries is the series terminating resistor.

Rseries > Rtrace - Rout

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF .
- A Ferrite Bead may be used to isolate the Board $V_{D D}$ from the clock generator $V_{D D}$ island. Ensure that the Ferrite Bead offers greater than $50 \Omega$ impedance at the clock frequency, under loaded DC conditions.
- If a Ferrite Bead is used, a $10 \mu \mathrm{~F}-22 \mu \mathrm{~F}$ tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.
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## IIC Serial Interface Information

The information in this section assumes familiarity with IIC programming.

## How to program ASM2I2310ANZ through IIC:

- Master (host) sends a start bit.
- Master (host) sends the write address D3 (H).
- ASM2I2310ANZ device will acknowledge.
- Master (host) sends the Command Byte.
- ASM2I2310ANZ device will acknowledge the Command Byte.
- Master (host) sends a Byte count
- ASM2I2310ANZ device will acknowledge the Byte count.
- Master (host) sends the Byte 0
- ASM2I2310ANZ device will acknowledge Byte 0
- Master (host) sends the Byte 1
- ASM2I2310ANZ device will acknowledge Byte 1
- Master (host) sends the Byte 2
- ASM2I2310ANZ device will acknowledge Byte 2
- Master (host) sends a Stop bit.

| Controller (Host) | ASM2I2310ANZ <br> (slave/receiver) |
| :--- | :---: |
| Start Bit |  |
| Slave Address D3(H) | ACK |
|  | ACK |
| Command Byte |  |
|  | ACK |
| Byte count |  |
|  | ACK |
| Byte 0 |  |
|  | ACK |
| Byte 1 |  |
|  | ACK |
| Byte 2 |  |
|  |  |
| Stop Bit |  |

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Package Information

## 28L SSOP Package (209 mil)



| Symbol | Dimensions |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Inches |  | Millimeters |  |
|  | Min | Max | Min | Max |
| A | $\ldots .$. | 0.079 | $\ldots$ | 2.0 |
| A1 | 0.002 | $\ldots$ | 0.05 | $\ldots$ |
| A2 | 0.065 | 0.073 | 1.65 | 1.85 |
| D | 0.394 | 0.409 | 10.00 | 10.40 |
| L | 0.021 | 0.037 | 0.55 | 0.95 |
| E | 0.295 | 0.319 | 7.50 | 8.10 |
| E1 | 0.197 | 0.220 | 5.00 | 5.60 |
| R1 | 0.004 | $\ldots$. | 0.09 | $\ldots .$. |
| b | 0.009 | 0.015 | 0.22 | 0.38 |
| b1 | 0.009 | 0.013 | 0.22 | 0.33 |
| c | 0.004 | 0.010 | 0.09 | 0.25 |
| c1 | 0.004 | 0.008 | 0.09 | 0.21 |
| L1 | $0.050 R E F$ |  | 1.25 REF |  |
| e | 0.026 BSC |  | 0.65 BSC |  |
| $\theta$ | $0^{\circ}$ | $8^{\circ}$ | $0^{\circ}$ | $8^{\circ}$ |

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## Ordering Information

| Part Number | Marking | Package Type | Operating Range |
| :--- | :--- | :--- | :---: |
| ASM2I2310ANZ-28-AT | 2I2310ANZ | 28-pin SSOP -Tube | Industrial |
| ASM2I2310ANZ-28-AR | 2I2310ANZ | 28-pin SSOP -Tape and Reel | Industrial |
| ASM2I2310AGNZ-28-AT | 2I2310AGNZ | 28-pin SSOP -Tube, Green | Industrial |
| ASM2I2310AGNZ-28-AR | 2I2310AGNZ | 28-pin SSOP -Tape and Reel, Green | Industrial |

## Device Ordering Information


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Note: This product utilizes US Patent \# 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003
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