Precision, Low Cost, High Speed, BiFET Op Amps

AD711/AD712/AD713

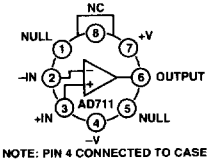
FEATURES
Enhanced Replacements for
TL081; TL082; TL084
LF411; LF412; LF347

AC PERFORMANCE
Settles to ±0.01% in 1.0 µs
16 V/µs min Slew Rate
3 MHz min Unity Gain Bandwidth
0.0003% Total Harmonic Distortion (THD)

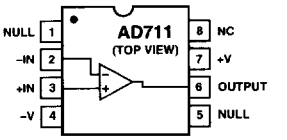
DC PERFORMANCE
Low Offset Voltages
(0.25 mV max—AD711C)
(0.30 mV max—AD712C)
(0.50 mV max—AD713K)
Low Offset Drift
(3 µV/°C max—AD711C)
(5 µV/°C max—AD712C)
200 V/mV min Open-Loop Gain
Low Noise (0.1 Hz to 10 Hz)
(4 µV p-p max—AD711C)
(4 µV p-p max—AD712C)
MIL-STD-883B Versions Available
Single: AD711
Dual: AD712
Quad: AD713

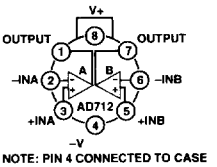
APPLICATIONS
Active Filters
Output Buffers for 12- and 14-Bit DACs
Input Buffers for Precision ADCs
Photo Diode Preamplifier Applications

CONNECTION DIAGRAMS

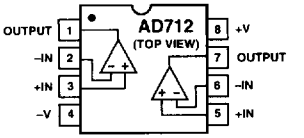


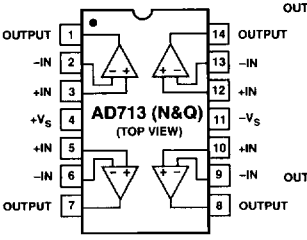
NOTE: PIN 4 CONNECTED TO CASE

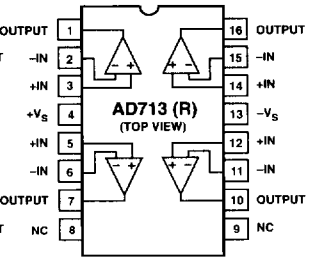




NOTE: PIN 4 CONNECTED TO CASE







NC = NO CONNECT

9

PRODUCT DESCRIPTION

The AD711/AD712/AD713 series are high speed, precision, monolithic operational amplifiers offering high performance at very modest prices. Their very low offset voltage and offset voltage drift are results of advanced laser wafer trimming technology. These benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of these op amps make them suitable for active filter designs. With a slew rate of 16 V/µs and settling times of 1 µs to 0.01%, the AD711/AD712/AD713 series is ideal for use as buffers for 12-bit D/A and A/D converters and as high speed integrators. The settling time is unmatched by any similar IC amplifier. The combination of excellent noise performance and low input current also make these amplifiers useful for photo diode preamplifiers. Common-mode rejection of 88 dB and open loop gain of 400 V/mV insure 12-bit performance even in high speed, unity gain, buffer circuits. These amplifiers are pinned out in standard op amp configurations and are available in various performance grades. The "J" and "K" grades are rated over the commercial temperature range of 0°C to +70°C. The "A," "B," and "C" grades are rated over the industrial temperature range of –40°C to +85°C. The "S" and "T" grades are rated over the military temperature range of –55°C to +125°C. Select versions are available processed to MIL-STD-883B, Rev. C or Standard Military Drawings.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

PRODUCT HIGHLIGHTS

1. The AD711/AD712/AD713 series offers excellent overall performance at competitive prices.
2. Analog Devices' advanced processing technology and 100% testing guarantees a low input offset voltage (0.25 mV max AD711C; 0.30 mV max AD712C). Input offset voltages are specified in the warmed up condition. Analog Devices' laser wafer drift trimming process reduces input offset voltage drifts to 3 µV/°C (AD711C) or 5 µV/°C (AD712C).
3. Along with precision dc performance, the AD711, AD712 and AD713 offer excellent dynamic response. They settle to ±0.01% in 1 µs and have a 100% tested minimum slew rate of 16 V/µs. This makes these parts ideal for DAC and ADC buffers, which require a combination of superior ac and dc performance.
4. Analog Devices' well matched, ion-implanted JFETs ensure low input bias currents and low input offset currents. Both input bias and offset currents are guaranteed in the warmed-up condition.

AD711/AD712/AD713–SPECIFICATIONS

AD711 (V_S = ±15 V @ T_A = +25°C unless otherwise noted)

Parameter	J/A/S Min	J/A/S Typ	J/A/S Max	K/B/T Min	K/B/T Typ	K/B/T Max	C Min	C Typ	C Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	2/1/1		0.2	0.5		0.10	0.25	mV
T_{MIN} to T_{MAX}			3/2/2			1.0			0.45	mV
vs. Temp		7	20/20/20		5	10		2	5	µV/°C
vs. Supply	76	95		80	100		86	110		dB
T_{MIN} to T_{MAX}	76/76/76			80			86			dB
Long-Term Stability		15			15			15		µV/Month
INPUT BIAS CURRENT[2]										
V_{CM} = 0 V		15	50		15	50		15	25	pA
V_{CM} = 0 V @ T_{MAX}			1.1/3.2/51			1.1/3.2/51			1.6	nA
V_{CM} = ±10 V		20	100		20	100		20	50	pA
INPUT OFFSET CURRENT										
V_{CM} = 0 V		10	25		5	25		5	10	pA
V_{CM} = 0 V @ T_{MAX}			0.6/1.6/26			0.6/1.6/26			0.65	nA
FREQUENCY RESPONSE										
Small Signal Bandwidth	3.0	4.0		3.4	4.0		3.4	4.0		MHz
Full Power Response		200			200			200		kHz
Slew Rate	16	20		18	20		18	20		V/µs
Settling Time to 0.01%		1.0	1.2		1.0	1.2		1.0	1.2	µs
Total Harmonic Distortion		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
Common Mode		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[3]		±20			±20			±20		V
Common-Mode Voltage[4]		+14.5, –11.5			+14.5, –11.5			+14.5, –11.5		
T_{MIN} to T_{MAX}	$-V_S$ + 4		$+V_S$ – 2	$-V_S$ + 4		$+V_S$ – 2	$-V_S$ + 4		$+V_S$ – 2	V
Common-Mode Rejection Ratio										
V_{CM} = ±10 V	76	88		80	88		86	94		dB
T_{MIN} to T_{MAX}	76/76/76	84		80	84		86	90		dB
V_{CM} = ±11 V	70	84		76	84		76	90		dB
T_{MIN} to T_{MAX}	70/70/70	80		74	80		74	84		dB
INPUT VOLTAGE NOISE		2			2			2	4	µV p-p
		45			45			45		nV/√Hz
		22			22			22		nV/√Hz
		18			18			18		nV/√Hz
		16			16			16		nV/√Hz
INPUT CURRENT NOISE		0.01			0.01			0.01		pA/√Hz
OPEN-LOOP GAIN	150	400		200	400		200	400		V/mV
	100/100/100			100			100			V/mV
OUTPUT CHARACTERISTICS										
Voltage	+13, –12.5	+13.9, –13.3		+13, –12.5	+13.9, –13.3		+13, –12.5	+13.9, –13.3		V
	±12/±12/±12	+13.8, –13.1		±12	+13.8, –13.1		±12	+13.8, –13.1		V
Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		2.5	3.4		2.5	3.0		2.5	2.8	mA

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.

[4]Typically exceeding –14.1 V negative common-mode voltage on either input results in an output phase reversal.

Specifications subject to change without notice.

AD712 (V_S = ±15 V @ T_A = +25°C unless otherwise noted)

Parameter	J/A/S Min	J/A/S Typ	J/A/S Max	K/B/T Min	K/B/T Typ	K/B/T Max	C Min	C Typ	C Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	3/1/1		0.2	1.0/0.7/0.7		0.1	0.3	mV
T_{MIN} to T_{MAX}			4/2/2			2.0/1.5/1.5			0.6	mV
vs. Temp		7	20/20/20		7	10		3	5	µV/°C
vs. Supply	76	95		80	100		86	110		dB
T_{MIN} to T_{MAX}	76/76/76			80			86			dB
Long-Term Stability		15			15			15		µV/Month
INPUT BIAS CURRENT[2]										
V_{CM} = 0 V		25	75		20	75		20	50	pA
V_{CM} = 0 V @ T_{MAX}		0.6/1.6/26	1.7/4.8/77		0.5/1.3/20	1.7/4.8/77		1.3	3.2	nA
V_{CM} = ±10 V			100			100			75	pA
INPUT OFFSET CURRENT										
V_{CM} = 0 V		10	25		5	25		5	10	pA
V_{CM} = 0 V @ T_{MAX}		0.3/0.7/11	0.6/1.6/26		0.1/0.3/5	0.6/1.6/26		0.3	0.7	nA
MATCHING CHARACTERISTICS										
Input Offset Voltage			3/1/1			1.0/0.7/0.7			0.3	mV
T_{MIN} to T_{MAX}			4/2/2			2.0/1.5/1.5			0.6	mV
Input Offset Voltage Drift			20/20/20			10			5	µV/°C
Input Bias Current			25			25			10	pA
Crosstalk @ f = 1 kHz		120			120			120		dB
@ f = 100 kHz		90			90			90		dB
FREQUENCY RESPONSE										
Small Signal Bandwidth	3.0	4.0		3.4	4.0		3.4	4.0		MHz
Full Power Response		200			200			200		kHz
Slew Rate	16	20		18	20		18	20		V/µs
Settling Time to 0.01%		1.0	1.2		1.0	1.2		1.0	1.2	µs
Total Harmonic Distortion		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE										
Differential		3×10^{12}‖5.5			3×10^{12}‖5.5			3×10^{12}‖5.5		Ω‖pF
Common Mode		3×10^{12}‖5.5			3×10^{12}‖5.5			3×10^{12}‖5.5		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[3]		±20			±20			±20		V
Common-Mode Voltage[4]		+14.5, –11.5			+14.5, –11.5			+14.5, –11.5		
T_{MIN} to T_{MAX}	$-V_S$ + 4		$+V_S$ – 2	$-V_S$ + 4		$+V_S$ –2	$-V_S$ + 4		$+V_S$ – 2	V
Common-Mode Rejection Ratio										
V_{CM} = ±10 V	76	88		80	88		86	94		dB
T_{MIN} to T_{MAX}	76/76/76	84		80	84		86	90		dB
V_{CM} = ±11 V	70	84		76	84		76	90		dB
T_{MIN} to T_{MAX}	70/70/70	80		74	80		74	84		dB
INPUT VOLTAGE NOISE		2			2			2		µV p-p
		45			45			45		nV/√Hz
		22			22			22		nV/√Hz
		18			18			18		nV/√Hz
		16			16			16		nV/√Hz
INPUT CURRENT NOISE		0.01			0.01			0.01		pA/√Hz
OPEN-LOOP GAIN	150	400		200	400		200	400		V/mV
	100/100/100			100			100			V/mV
OUTPUT CHARACTERISTICS										
Voltage	+13, –12.5	+13.9, –13.3		+13, –12.5	+13.9, –13.3		+13, –12.5	+13.9, –13.3		V
	±12/±12/±12	+13.8, –13.1		±12	+13.8, –13.1		±12	+13.8, –13.1		V
Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		5.0	6.8		5.0	6.0		5.0	5.6	mA

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[3]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.
[4]Typically exceeding –14.1 V negative common-mode voltage on either input results in an output phase reversal.

Specifications subject to change without notice.

REV. 0

AD711/AD712/AD713–SPECIFICATIONS

AD713 (V_S = ±15 V @ T_A = +25°C unless otherwise noted)

Parameter	Conditions	J/A/S Min	J/A/S Typ	J/A/S Max	K/B/T Min	K/B/T Typ	K/B/T Max	Units
INPUT OFFSET VOLTAGE[1]								
Initial Offset			0.3	**1.5**		0.2	**0.5**	mV
Offset	T_{MIN} to T_{MAX}		0.5	2/2/2		0.4	**0.7/0.7/1.0**	mV
vs. Temp			5			5	20/**20**/**15**	µV/°C
vs. Supply		**78**	95		**84**	100		dB
vs. Supply	T_{MIN} to T_{MAX}	76/76/**76**	95		**84**	100		dB
Long-Term Stability			15			15		µV/
Month								
INPUT BIAS CURRENT[2]	V_{CM} = 0 V		40	**150**		40	**75**	pA
	V_{CM} = 0 V @ T_{MAX}			3.4/9.6/154			1.7/4.8/77	nA
	V_{CM} = ±10 V		55	200		55	**120**	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		10	**75**		10	**35**	pA
	V_{CM} = 0 V @ T_{MAX}			1.7/4.8/77			0.8/2.2/36	nA
MATCHING CHARACTERISTICS								
Input Offset Voltage			0.5	**1.8**		0.4	**0.8**	mV
Input Offset Voltage	T_{MIN} to T_{MAX}		0.7	2.3/2.3/**2.3**		0.6	**1.0/1.0/1.3**	mV
Input Offset Voltage Drift			8			6	25	µV/°C
Input Bias Current			10	**100**		10	**35**	pA
Crosstalk	f = 1 kHz			–130			–130	dB
	f = 100 kHz			–95			–95	dB
FREQUENCY RESPONSE								
Small Signal Bandwidth	Unity Gain	3.0	4.0		3.4	4.0		MHz
Full Power Response	V_O = 20 V p-p		200			200		kHz
Slew Rate	Unity Gain	**16**	20		**18**	20		V/µs
Settling Time to 0.01%			1.0	1.2		1.0	1.2	µs
Total Harmonic Distortion	f = 1 kHz; $R_L \geq 2$ kΩ; V_O = 3 V rms		0.0003			0.0003		%
INPUT IMPEDANCE								
Differential			$3\times10^{12}\|\|5.5$			$3\times10^{12}\|\|5.5$		Ω‖pF
Common Mode			$3\times10^{12}\|\|5.5$			$3\times10^{12}\|\|5.5$		Ω‖pF
INPUT VOLTAGE RANGE								
Differential[3]			±20			±20		V
Common-Mode Voltage[4]			+14.5, –11.5			+14.5, –11.5		V
	T_{MIN} to T_{MAX}	–11		+13	**–11**		+13	V
Common Mode	V_{CM} = ±10 V	**78**	88		**84**	94		dB
Rejection Ratio	T_{MIN} to T_{MAX}	76/76/**76**	84		**82**	90		dB
	V_{CM} = ±11 V	**72**	84		**78**	90		dB
	T_{MIN} to T_{MAX}	70/70/**70**	80		**74**	84		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		2			2		µV p-p
	f = 10 Hz		45			45		nV/√Hz
	f = 100 Hz		22			22		nV/√Hz
	f = 1 kHz		18			18		nV/√Hz
	f = 10 kHz		16			16		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.01			0.01		pA/√Hz
OPEN-LOOP GAIN	V_O = ±10 V; $R_L \geq 2$ kΩ	**150**	400		**200**	400		V/mV
	T_{MIN} to T_{MAX}	100/100/**100**			**100**			V/mV
OUTPUT CHARACTERISTICS								
Voltage	$R_L \geq 2$ kΩ	+13, –12.5	+13.9, –13.3		+13, –12.5	+13.9, –13.3		V
	T_{MIN} to T_{MAX}	±12/±12/**±12**	+13.8, –13.1		**±12**	+13.8, –13.1		V
Current	Short Circuit		25			25		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			10.0	**13.5**		10.0	**12.0**	mA
TRANSISTOR COUNT	# of Transistors		120			120		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.

[4]Typically exceeding –14.1 V negative common-mode voltage on either input results in an output phase reversal.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Internal Power Dissipation[2]
Input Voltage ..... $\pm V_S$
Differential Input Voltage ..... $+V_S$ and $-V_S$
Output Short Circuit Duration (Single Amplifier) ... Indefinite
Storage Temperature Range (N, R) .....–65°C to +125°C
Storage Temperature Range (Q) .....–65°C to +150°C
Operating Temperature Range
AD71xJ/K .....0°C to +70°C
AD71xA/B .....–40°C to +85°C
AD71xS/T .....–55°C to +125°C
Lead Temperature Range (Soldering 60 sec) ..... +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:

8-Pin Plastic Package	θ_{JA} = 165°C/Watt
8-Pin Cerdip Package	θ_{JA} = 110°C/Watt
8-Pin Metal Can Package	θ_{JA} = 150°C/Watt
8-Pin Small Outline Package	θ_{JA} = 155°C/Watt
14-Pin Plastic Package	θ_{JA} = 150°C/Watt
14-Pin Cerdip Package	θ_{JA} = 110°C/Watt
16-Pin SOIC Package	θ_{JA} = 100°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD711AH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD711AQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD711BH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD711BQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD711CH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD711CQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD711JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD711JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711JR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711JR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711KN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD711KR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711KR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711KR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711SCHIPS	–55°C to +125°C	Bare Die	
AD711SQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD711TQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD712ACHIPS	–40°C to +85°C	Bare Die	
AD712AH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD712AQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD712BH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD712BQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD712CH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD712CQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD712JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD712JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712JR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712JR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712KN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD712KR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712KR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712KR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712SCHIPS	–55°C to +125°C	Bare Die	
AD712SQ	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD712SQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD712TQ	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD712TQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD713AQ	–40°C to +85°C	14-Pin Ceramic DIP	Q-14
AD713BQ	–40°C to +85°C	14-Pin Ceramic DIP	Q-14
AD713JCHIPS	0°C to +70°C	Bare Die	
AD713JN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD713JR-16	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713JR-16-REEL	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713JR-16-REEL7	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713KN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD713SCHIPS	–55°C to +125°C	Bare Die	
AD713SQ	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713SQ/883B	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713TQ	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713TQ/883B	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
5962-9063301MCA	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
5962-9063302MCA	–55°C to +125°C	14-Pin Ceramic DIP	Q-14

*For outline information see Package Information section.

9