HFBR-5921L/HFBR-5923L

Fibre Channel 2.125/1.0625 GBd 850 nm
Small Form Factor Pin Through Hole (PTH)
Low Voltage (3.3 V) Optical Transceiver

Data Sheet

Description

The HFBR-5921L/5923L optical transceivers from Avago Technologies offer maximum flexibility to Fibre Channel designers, manufacturers, and system integrators to implement a range of solutions for multi-mode Fibre Channel applications. This product is fully compliant with all equipment meeting the Fibre Channel FC-PI 200-M5-SN-I and 200-M6-SN-I 2.125 GBd specifications, and is compatible with the Fibre Channel FC-PI 100-M5-SN-I, FC-PI 100-M6-SN-I, FC-PH2 100-M5-SN-I, and FC-PH2 100-M6-SN-I 1.0625 GBd specifications. The HFBR-5921L/5923L is also compliant with the SFF Multi Source Agreement (MSA).

Module Package

Avago offers the industry two Pin Through Hole package options utilizing an integral LC-Duplex optical interface connector. Both transceivers use a reliable 850 nm VCSEL source and requires a 3.3 V DC power supply for optimal system design.

Related Products

- HFBR-5602: 850 nm +5 V Gigabit Interface Converter (GBIC) for Fiber Channel FC-PH-2
- HFBR-53D3: 850 nm +5 V 1 x 9 Laser transceiver for Fiber Channel FC-PH-2
- HFBR-5910E: 850 nm +3.3 V SFF MTRJ Laser transceiver for Fibre Channel FC-PH-2
- HDMP-2630/2631: 2.125/1.0625 Gbps TRx family of SerDes IC
- HFBR-5720L: 850 nm 3.3 V 2.125/1.0625 Gbps SFP Transceiver

Features

- Compliant with 2.125 GBd Fibre Channel FC-PI standard
  – FC-PI 200-M5-SN-I for 50/125 mm multimode cables
  – FC-PI 200-M6-SN-I for 62.5/125 mm multimode cables
- Compliant with 1.0625 GBd VCSEL operation for both 50/125 and 62.5/125 mm multimode cables
- Industry standard Pin Through Hole (PTH) package
- LC-duplex connector optical interface
- Link lengths at 2.125 GBd:
  0.5 to 300 m – 50/125 mm MMF
  0.5 to 150 m – 62.5/125 mm MMF
- Link lengths at 1.0625 GBd:
  0.5 to 500 m – 50/125 mm MMF
  0.5 to 300 m – 62.5/125 mm MMF
- Reliable 850 nm Vertical Cavity Surface Emitting Laser (VCSEL) source technology
- Laser AEL Class I (eye safe) per:
  US 21 CFR (J)
  EN 60825-1 (+All)
- Single +3.3 V power supply operation
- 2 x 5 or 2 x 6 DIP package style with LC-duplex fiber
- Wave solder and aqueous wash process compatible

Applications

- Mass storage system I/O
- Computer system I/O
- High speed peripheral interface
- High speed switching systems
- Host adapter I/O
- RAID cabinets

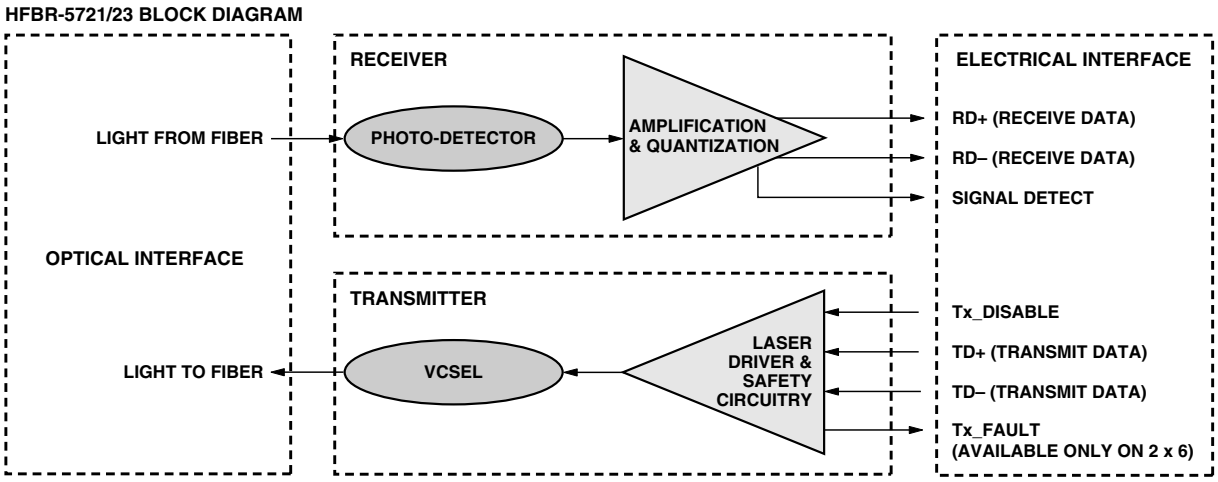


Figure 1. Transceiver functional diagram.

See Table 5 for Process Compatibility Specifications.

Module Diagrams

Figure 1 illustrates the major functional components of the HFBR-5921/5923. The connection diagram for both modules are shown in Figure 2. Figure 7 depicts the external configuration and dimensions of the module.

Installation

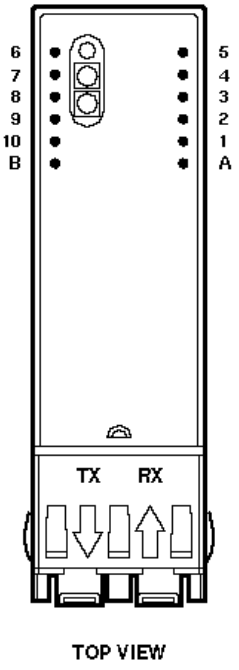
The HFBR-5921L/5923L can be installed in any MSA-compliant Pin Through Hole port. The module Pin Description is shown in Figure 2.

Solder and Wash Process Capability

These transceivers are delivered with protective process plugs inserted into the LC connector receptacle. This process plug protects the optical subassemblies during wave solder and aqueous wash processing and acts as a dust cover during shipping. These transceivers are compatible with industry standard wave or hand solder processes.

Recommended Solder Fluxes

Solder fluxes used with the HFBR-5921L/5923L should be water-soluble, organic fluxes. Recommended solder fluxes include Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alpha-Metals of Jersey City, NJ.



PIN DESCRIPTION		
PIN	NAME	TYPE
1	Rx GROUND	GROUND
2	Rx POWER	POWER
3	Rx SD	STATUS OUT
4	Rx DATA BAR	SIGNAL OUT
5	Rx DATA	SIGNAL OUT
6	Tx POWER	POWER
7	Tx GROUND	GROUND
8	Tx DISABLE	CONTROL IN
9	Tx DATA	SIGNAL IN
10	Tx DATA BAR	SIGNAL IN
A	N/C (2 x 6 ONLY)	NOT CONNECTED
B	Tx FAULT (2 x 6 ONLY)	STATUS OUT

Figure 2. Module pin assignments and pin configuration.

Recommended Cleaning/Degreasing Chemicals

Alcohols: methyl, isopropyl, isobutyl.

Aliphatics: hexane, heptane.

Other: naphtha. Do not use partially halogenated hydrocarbons such as 1,1.1 trichoroethane or ketones such as MEK, acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrolldone. Also, Avago does not recommend the use of cleaners that use halogenated hydrocarbons because of their potential environmental harm.

Transmitter Section

The transmitter section includes the transmitter optical subassembly (TOSA) and laser driver circuitry. The TOSA, containing an 850 nm VCSEL (Vertical Cavity Surface Emitting Laser) light source, is located at the optical interface and mates with the LC optical connector. The TOSA is driven by a custom silicon IC, which converts differential logic signals into an analog laser diode drive current. This TX driver circuit regulates the optical power at a constant level provided the data pattern is valid 8B/10B DC balanced code.

TX Disable

The HFBR-5921L/5923L accepts a transmit disable control signal input which shuts down the transmitter. A high signal implements this function while a low signal allows normal laser operation. In the event of a fault (e.g., eye safety circuit activated), cycling this control signal resets the module. The TX Disable control should be actuated upon initialization of the module. See Figure 6 for product timing diagrams.

TX Fault (Available only on the 2 x 6)

The HFBR-5923L module features a transmit fault control signal output which when high indicates a laser transmit fault has occurred and when low indicates normal laser operation. A transmitter fault condition can be caused by deviations from the recommended module operating conditions or by violation of eye safety conditions. A transient fault can be cleared by cycling the TX Disable control input.

Eye Safety Circuit

For an optical transmitter device to be eye-safe in the event of a single fault failure, the transmitter will either maintain normal, eye-safe operation or be disabled. In the event of an eye safety fault, the VCSEL will be disabled.

Receiver Section

The receiver section includes the receiver optical subassembly (ROSA) and amplification/quantization circuitry. The ROSA, containing a PIN photodiode and custom transimpedance preamplifier, is located at the optical interface and mates with the LC optical connector. The ROSA is mated to a custom IC that provides post-amplification and quantization. This circuit also includes a Signal Detect (SD) circuit which provides an LVTTLcompatible logic low output in the absence of a usable input optical signal level.

Signal Detect

The Signal Detect (SD) output indicates if the optical input signal to the receiver does not meet the minimum detectable level for Fibre Channel compliant signals. When SD is low it indicates loss of signal. When SD is high it indicates normal operation. The Signal Detect thresholds are set to indicate a definite optical fault has occurred (e.g., disconnected or broken fiber connection to receiver, failed transmitter).

Functional Data I/O

Avago's HFBR-5921L/5923L fiber-optic transceiver is designed to accept industry standard differential signals. In order to reduce the number of passive components required on the customer's board, Avago has included the functionality of the transmitter bias resistors and coupling capacitors within the fiber optic module. The transceiver is compatible with an "AC-coupled" configuration and is internally terminated. Figure 1 depicts the functional diagram of the HFBR- 5921/5923.

Caution should be taken to account for the proper interconnection between the supporting Physical Layer integrated circuits and the HFBR-5921L/5923L . Figure 4 illustrates the recommended interface circuit.

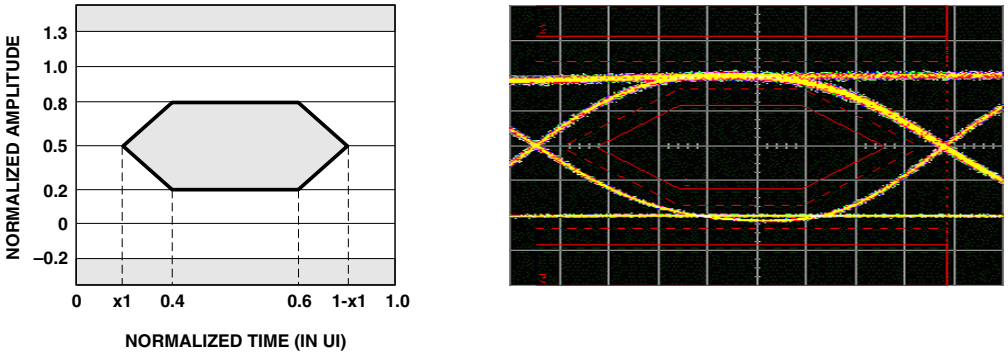


Figure 3. Transmitter eye mask diagram and typical transmitter eye.

Application Support

Evaluation Kit

To help you in your preliminary transceiver evaluation, Avago offers a 2.125 GBd Fibre Channel evaluation board. This board will allow testing of the HFBR-5921L/ 5923L optical transceivers. Please contact your local field sales representative for availability and ordering details.

Reference Designs

Reference designs for the HFBR-5921L/5923L fiber-optic transceiver and the HDMP-2630/2631 physical layer IC are available to assist the equipment designer. Figure 4 depicts a typical application configuration, while Figure 5 depicts the multisourced power supply filter circuit design. All artwork is available at the Avago electronic bulletin board. Please contact your local field sales engineer for more information regarding application tools.

Regulatory Compliance

See Table 1 for transceiver Regulatory Compliance performance. The overall equipment design will determine the certification level. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

There are two conditions in which immunity to ESD damage is important. Table 1 documents our immunity to both of these conditions. The first condition is during handling of the transceiver prior to attachment to the PCB. To protect the transceiver, it is important to use normal ESD handling precautions. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas. The ESD sensitivity of the HFBR-5921L/5923L is compatible with typical industry production environments. The second condition is static discharges to the exterior of the host equipment chassis after installation. To the extent that the duplex LC optical interface is exposed to the outside of the host equipment chassis, it may be subject to system-level ESD requirements. The ESD performance of the HFBR-5921L/5923L exceeds typical industry standards.

Immunity

Equipment hosting the HFBR-5921L/5923L modules will be subjected to radio-frequency electromagnetic fields in some environments. The transceivers have good immunity to such fields due to their shielded design.

Table 1. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Class 2 (> 2000 V)
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	Variation of IEC 61000-4-2	Typically withstand at least 25 kV without damage when the duplex LC connector receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22A) VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows a negligible effect from a 10 V/m field swept from 80 to 1000 MHz applied to the transceiver without a chassis enclosure.
Eye Safety	US FDA CDRH AEL Class 1 EN(IEC)60825-1,2, EN60950 Class 1	CDRH file # 9720151-13 TUV file # E9971086.06[1]
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment.	UL file # E173874

Note:

1. Changes to IEC 60825-1,2 are currently anticipated to allow higher eye-safe Optical Output Power levels. Agilent may choose to take advantage of these changes at a later date.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago Technologies will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. The metal housing and shielded design of the HFBR-5921L/5923L minimize the EMI challenge facing the host equipment designer. These transceivers provide superior EMI performance. This greatly assists the designer in the management of the overall system EMI performance.

Eye Safety

These 850 nm VCSEL-based transceivers provide Class 1 eye safety by design. Avago Technologies has tested the transceiver design for compliance with the requirements listed in Table 1: Regulatory Compliance, under normal operating conditions and under a single fault condition.

Flammability

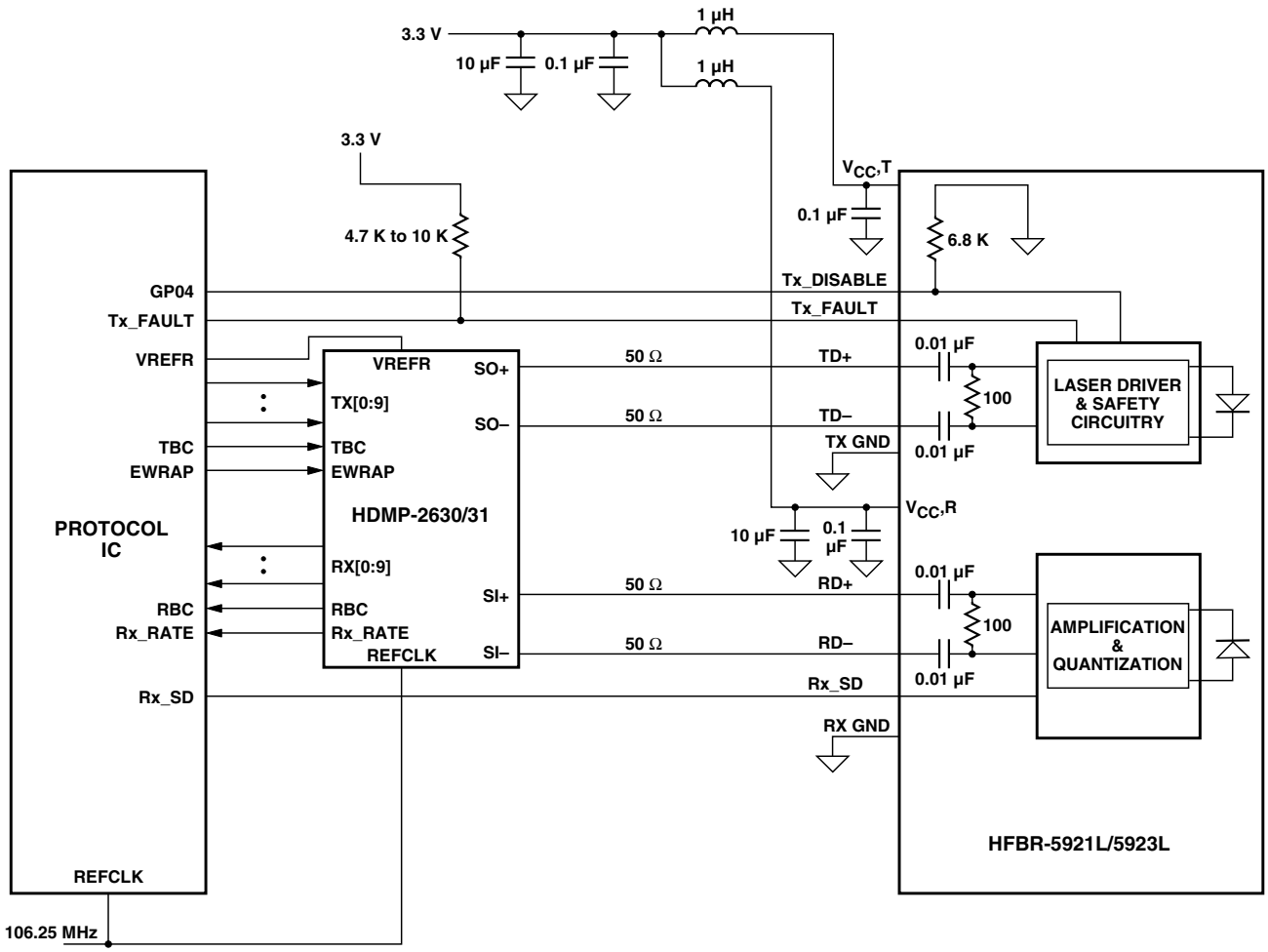
The HFBR-5921L/5923L VCSEL transceiver housing is made of metal and high strength, heat resistant, chemically resistant, and UL 94V-0 flame retardant plastic.

Caution

There are no user serviceable parts nor is any maintenance required for the HFBR-5921/5923. All adjustments are made at the factory before shipment to our customers. Tampering with or modifying the performance of the HFBR-5921L/5923L will result in voided product warranty. It may also result in improper operation of the HFBR-5921L/5923L circuitry, and possible overstress of the laser source. Device degradation or product failure may result. Connection of the HFBR-5921L/5923L to a nonapproved optical source, operating above the recommended absolute maximum conditions or operating the HFBR-5921L/5923L in a manner inconsistent with its design and function may result in hazardous radiation exposure and may be considered an act of modifying or manufacturing a laser product. The person(s) performing such an act is required by law to re-certify and re-identify the laser product under the provisions of U.S. 21 CFR (Subchapter J) and the TUV.

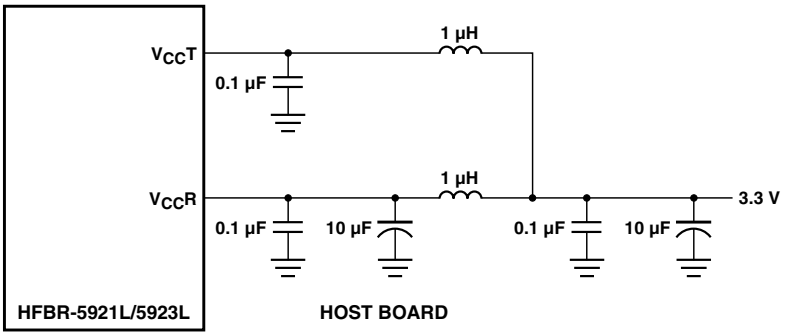
Ordering Information

Please contact your local field sales engineer or one of Avago Technologies franchised distributors for ordering information. For technical information regarding this product, including the MSA, please visit Avago Technologies Website at www.avagotech.com/



NOTE: Tx_FAULT REQUIRED FOR 2 x 6 MODULE ONLY.

Figure 4. Typical application configuration.



NOTE: INDUCTORS MUST HAVE LESS THAN 1 Ω SERIES RESISTANCE PER MSA.

Figure 5. MSA recommended power supply filter.

Table 2. Pin Description

Pin	Name	Function/Description	MSA Notes
1	$V_{EE}R$	Receiver Ground	1
2	$V_{CC}R$	Receiver Power –3.3 V ±5%	6
3	SD	Signal Detect – Low indicates Loss of Signal	4
4	RD–	Inverse Received Data Out	5
5	RD+	Received Data Out	5
6	$V_{CC}T$	Transmitter Power –3.3 V ±5%	6
7	$V_{EE}T$	Transmitter Ground	1
8	TX Disable	Transmitter Disable – Module disables on High	3
9	TD+	Transmitter Data In	7
10	TD–	Inverse Transmitter Data In	7
A	N/C (2 x 6 Only)	Not Connected	
B	TX Fault (2 x 6 Only)	Transmitter Fault Indication – High indicates a Fault	2

Notes:

1. Transmitter and Receiver Ground are common in the internal module PCB. They are electrically connected to signal ground within the module, and to the housing shield (see Note 5 in Figure 7c). This housing shield is electrically isolated from the nose shield which is connected to chassis ground (see Note 4 in Figure 7c).
2. TX Fault is an open collector/drain output, which should be pulled up externally with a 4.7 K – 10 KΩ resistor on the host board to a supply < $V_{CC}T$ + 0.3 V or $V_{CC}R$ + 0.3 V. When high, this output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to < 0.8 V.
3. TX disable input is used to shut down the laser output per the state table below. It is pulled down internally within the module with a 6.8 KΩ resistor.

Low (0 – 0.8 V):	Transmitter on
Between (0.8 V and 2.0 V):	Undefined
High (2.0 – 3.465 V):	Transmitter Disabled
Open:	Transmitter Enabled

4. SD (Signal Detect) is a normally high LVTTL output. When high it indicates that the received optical power is adequate for normal operation. When Low, it indicates that the received optical power is below the worst case receiver sensitivity, a fault has occurred, and the link is no longer valid. SD is pulled up internally with a 2 KΩ resistor to $V_{CC}R$.
5. RD-/+: These are the differential receiver outputs. They are AC coupled 100 Ω differential lines which should be terminated with 100 Ω differential at the user SerDes. The AC coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 400 and 2000 mV differential (200 – 1000 mV single ended) when properly terminated. These levels are compatible with CML and LVPECL voltage swings.
6. $V_{CC}R$ and $V_{CC}T$ are the receiver and transmitter power supplies. They are defined as 3.135 – 3.465 V at the PTH connector pin. The maximum supply current is 200 mA.
7. TD-/+: These are the differential transmitter inputs. They are AC coupled differential lines with 100 Ω differential termination inside the module. The AC coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swings of 400 – 2400 mV (200 – 1200 mV single ended), though it is recommended that values between 400 and 1200 mV differential (200 – 600 mV single ended) be used for best EMI performance. These levels are compatible with CML and LVPECL.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Storage Temperature	T_S	–40		+100	°C	1
Case Temperature	T_C	0		+85	°C	1, 2
Relative Humidity	RH	5		95	%	1
Supply Voltage	V_{CC}T,R	–0.5		3.6	V	1, 2
Data/Control Input Voltage	V_I	–0.5		V_{CC} + 0.3	V	1
Sense Output Current – SD,TX Fault	I_D			150	mA	1

Notes:
1. Absolute Maximum Ratings are those values beyond which damage to the device may occur if these limits are exceeded for other than a short period of time. See Reliability Data Sheets for specific reliability performance.
2. Between Absolute Maximum Ratings and the Recommended Operating Conditions, functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time.

Table 4. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Case Temperature	T_C	0		70	°C	1
Module Supply Voltage	V_{CC}T,R	3.135	3.3	3.465	V	1
Data Rate Fibre Channel			1.0625 2.125		Gb/s	1

Notes:
1. Recommended operating conditions are those values outside of which functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time. See Reliability Data Sheet for specific reliability performance.

Table 5. Process Compatibility

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Hand Lead Solder Temperature/Time	T_{SOLD}/t_{SOLD}		+260/10	°C/sec	
Wave Solder and Aqueous Wash	T_{SOLD}/t_{SOLD}		+260/10	°C/sec	1

Note:
1. Aqueous wash pressure < 110 psi.

Table 6. Transceiver Electrical Characteristics
(T_C = 0°C to 70°C, $V_{CC}T,R$ = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
AC Electrical Characteristics						
Power Supply Noise Rejection (Peak-to-Peak)	PSNR		100		mV	1
DC Electrical Characteristics						
Module Supply Current	I_{CC}		133	200	mA	
Power Dissipation	P_{DISS}		440	693	mW	
Sense Output:						
Transmit Fault [TX_FAULT],	V_{OH}	2.0		$V_{CC}T,R$ + 0.3	V	2
2 x 6 Only	V_{OL}			0.8	V	
Sense Output:						
Signal Detect [SD]	V_{OH}	2.4		$V_{CC}T,R$ + 0.3	V	3
	V_{OL}			0.4	V	
Control Inputs:						
Transmitter Disable	V_{IH}	2.0		V_{CC} + 0.3	V	
[TX_DISABLE]	V_{IL}	0		0.8	V	

Notes:
1. MSA filter is required on host board 10 Hz to 2 MHz.
2. External 4.7-10 KΩ pull-up resistor required for TX_Fault.
3. SD pin is pulled up internally with a 2 KΩ resistor to $V_{CC}R$.

Table 7. Transmitter and Receiver Electrical Characteristics
(T_C = 0°C to 70°C, $V_{CC}T,R$ = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Data Input:						
Transmitter Differential Input Voltage (TD +/–)	V_I	400		2400	mV	1
Data Output:						
Receiver Differential Output Voltage (RD +/–)	V_O	400	735	2000	mV	2
Contributed Deterministic	DJ			0.1	UI	3, 6
Jitter (Receiver) 2.125 Gb/s				47	ps	
Contributed Deterministic	DJ			0.12	UI	3, 6
Jitter (Receiver) 1.0625 Gb/s				113	ps	
Contributed Random Jitter	RJ			0.162	UI	4, 6
(Receiver) 2.125 Gb/s				76	ps	
Contributed Random Jitter	RJ			0.098	UI	4, 6
(Receiver) 1.0625 Gb/s				92	ps	
Receive Data Rise and Fall Times (Receiver)	Trf			250	ps	5

Notes:
1. Internally AC coupled and terminated (100 Ohm differential). These levels are compatible with CML and LVPECL voltage swings.
2. Internally AC coupled with an external 100 ohm differential load termination.
3. Contributed DJ is measured on an oscilloscope in average mode with 50% threshold and K28.5 pattern.
4. Contributed RJ is calculated for $1x10^{-12}$ BER by multiplying the RMS jitter (measured on a single rise or fall edge) from the oscilloscope by 14. Per the FC-PI standard (Table 13 - MM jitter output, Note 1), the actual contributed RJ is allowed to increase above its limit if the actual contributed DJ decreases below its limits, as long as the component output DJ and TJ remain within their specified FC-PI maximum limits with the worst case specified component jitter input.
5. 20%-80% Rise and Fall times measured with a 500 MHz signal utilizing a 1010 data pattern.
6. In a network link, each component's output jitter equals each component's input jitter combined with each component's contributed jitter. Contributed DJ adds in a linear fashion and contributed RJ adds in a RMS fashion. In the Fibre Channel FC-PI Rev 11 specification "6.3.3 MM jitter budget" section, there is a table specifying the input and output DJ and TJ for the receiver at each data rate. In that table, RJ is found from TJ - DJ where the RX input jitter is noted as Gamma R and the RX output jitter is noted as Delta R. Our component contributed jitter is such that, if the maximum specified input jitter is present, and is combined with our maximum contributed jitter, then we meet the specified maximum output jitter limits listed in the FC-PI MM jitter specification table.

Table 8. Transmitter Optical Characteristics
(TC = 0°C to 70°C, $V_{CC}T,R$ = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Output Optical Power (Average)	P_{OUT}	–10	–6.3	0	dBm	50/125 µm NA = 0.2 Note 1
	P_{OUT}	–10	–6.2	0	dBm	62.5/125 µm NA = 0.275 Note 1
Optical Extinction Ratio	ER		9		dB	
Optical Modulation Amplitude (Peak-to-Peak) 2.125 Gb/s	OMA	196	392		uW	FC-PI Std Note 2
Optical Modulation Amplitude (Peak-to-Peak) 1.0625 Gb/s	OMA	156	350		uW	FC-PI Std Note 3
Center Wavelength	λ_C	830		860	nm	FC-PI Std
Spectal Width – rms	σ			0.85	nm	FC-PI Std
Optical Rise /Fall Time	$T_{rise/fall}$			150	ps	20%–80%, FC-PI Std
RIN_{12}(OMA), maximum	RIN			–117	dB/Hz	FC-PI Std
Contributed Deterministic Jitter (Transmitter) 2.125 Gb/s	DJ			0.12	UI	4, 5
				56	ps	
Contributed Deterministic Jitter (Transmitter) 1.0625 Gb/s	DJ			0.09	UI	4, 6
				85	ps	
Contributed Random Jitter (Transmitter) 2.125 Gb/s	RJ			0.134	UI	5, 6
				63	ps	
Contributed Random Jitter (Transmitter) 1.0625 Gb/s	RJ			0.177	UI	5, 6
				167	ps	
P_{OUT} TX_DISABLE Asserted	P_{OFF}			–35	dBm	

Notes:
1. Max P_{out} is the lesser of 0 dBm or Maximum allowable per Eye Safety Standard.
2. An OMA of 196 is approximately equal to an average power of –9 dBm assuming an Extinction Ratio of 9 dB.
3. An OMA of 156 is approximately equal to an average power of –10 dBm assuming an Extinction Ratio of 9 dB.
4. Contributed DJ is measured on an oscilloscope in average mode with 50% threshold and K28.5 pattern.
5. Contributed RJ is calculated for $1x10^{-12}$ BER by multiplying the RMS jitter (measured on a single rise or fall edge) from the oscilloscope by 14. Per the FC-PI standard (Table 13 - MM jitter output, note 1), the actual contributed RJ is allowed to increase above its limit if the actual contributed DJ decreases below its limits, as long as the component output DJ and TJ remain within their specified FC-PI maximum limits with the worst case specified component jitter input.
6. In a network link, each component's output jitter equals each component's input jitter combined with each component's contributed jitter. Contributed DJ adds in a linear fashion and contributed RJ adds in a RMS fashion. In the Fibre Channel FC-PI Rev 11 specification "6.3.3 MM jitter budget" section, there is a table specifying the input and output DJ and TJ for the transmitter at each data rate. In that table, RJ is found from TJ – DJ, where the TX input jitter is noted as Delta T, and the TX output jitter is noted as Gamma T. Our component contributed jitter is such that, if the maximum specified input jitter is present, and is combined with our maximum contributed jitter, then we meet the specified maximum output jitter limits listed in the FC-PI MM jitter specification table.

Table 9. Receiver Optical Characteristics
(TC = 0°C to 70°C, $V_{CC}T,R$ = 3.3 V ± 5%)

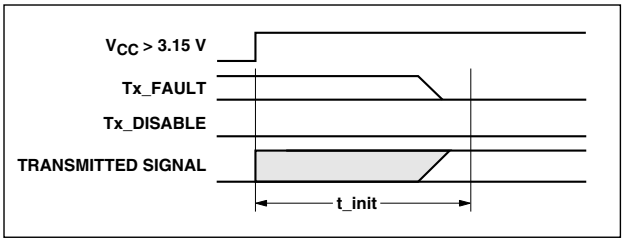
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Optical Power	PIN			0	dBm	FC-PI Std
Min Optical Modulation Amplitude (Peak-to-Peak) 2.125 Gb/s	OMA	49	16		µW	FC-PI Std Note 1
Min Optical Modulation Amplitude (Peak-to-Peak) 1.0625 Gb/s	OMA	31	18		µW	FC-PI Std Note 2
Stressed Receiver Sensitivity (OMA) 2.125 Gb/s		96	33		µW	50 µm fiber, FC-PI Std
		109	25		µW	62.5 µm fiber, FC-PI Std Note 3
Stressed Receiver Sensitivity (OMA) 1.0625 Gb/s		55	19		µW	50 µm fiber, FC-PI Std
		67	16		µW	62.5 µm fiber, FC-PI Std Note 4
Return Loss		12			dB	FC-PI Std
Signal Detect – De-Assert	P_D	–31		–17.5	dBm	Note 5
Signal Detect – Assert	P_A			–17.0	dBm	Note 5
Signal Detect Hysteresis	$P_A – P_D$	0.5	2.3	5	dB	

Notes:
1. An OMA of 49 uW is approximately equal to an average power of -15dBm, and the OMA typical of 16 uW is approximately equal to an average power of -20 dBm, assuming an Extinction Ratio of 9dB. Sensitivity measurements are made at eye center with BER = $10E^{-12}$.
2. An OMA of 31 is approximately equal to an average power of –17 dBm assuming an Extinction Ratio of 9 dB.
3. 2.125 Gb/s Stressed receiver vertical eye closure penalty (ISI) min is 1.26 dB for 50 µm fiber and 2.03 dB for 62.5 µm fiber. Stressed receiver DCD component min (at TX) is 40 ps.
4. 1.0625 Gb/s Stressed receiver vertical eye closure penalty (ISI) min is 0.96 dB for 50 µm fiber and 2.18 dB for 62.5 µm fiber. Stressed receiver DCD component min (at TX) is 80 ps.
5. These average power values are specified with an Extinction Ratio of 9dB. The Signal Detect circuitry responds to OMA (peak-to-peak) power, not to average power.

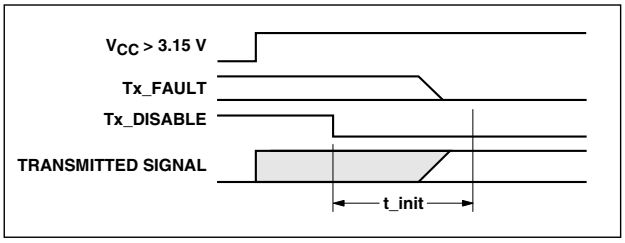
Table 10. Transceiver Timing Characteristics
(TC = 0°C to 70°C, $V_{CC}T,R$ = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Maximum	Unit	Notes
TX Disable Assert Time	t_off		10	µs	1
TX Disable Negate Time	t_on		1	ms	2
Time to Initialize, including Reset of TX_Fault	t_init		300	ms	3
TX Fault Assert Time (2 x 6 Module only)	t_fault		100	µs	4, 8
TX Disable to Reset	t_reset	10		µs	5
SD Assert Time	t_loss_on		100	µs	6
SD De-assert Time	t_loss_off		100	µs	7

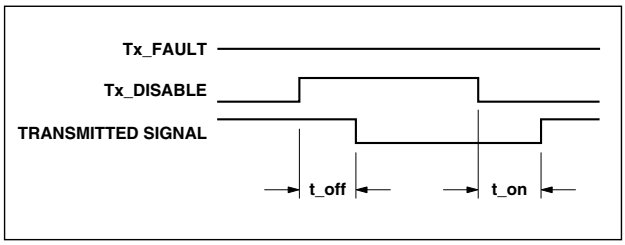
Notes:
1. Time from rising edge of TX Disable to when the optical output falls below 10% of nominal.
2. Time from falling edge of TX Disable to when the modulated optical output rises above 90% of nominal.
3. From power on or negation of TX Fault using TX Disable.
4. Time from fault to TX fault on.
5. Time TX Disable must be held high to reset TX_FAULT.
6. Time from LOS state to RX LOS assert.
7. Time from non-LOS state to RX LOS de-assert.
8. TX_Fault is only available on the 2 x 6 option – HFBR-5923L.



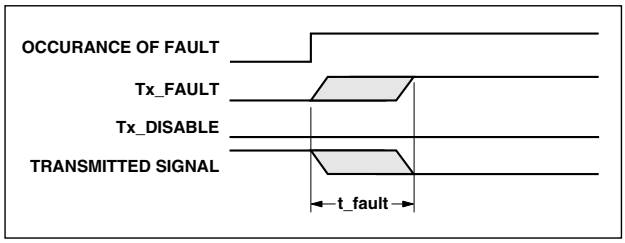
t-init: TX DISABLE DE-ASSERTED



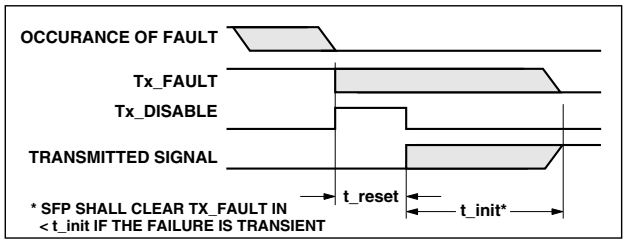
t-init: TX DISABLE ASSERTED



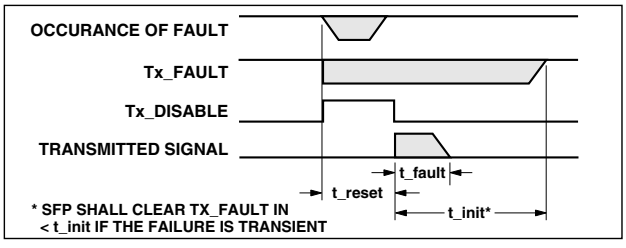
t-off & t-on: TX DISABLE ASSERTED THEN NEGATED



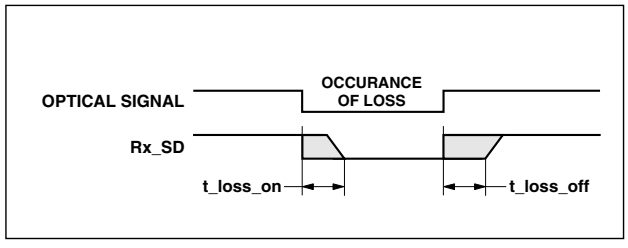
t-fault (2 x 6 only): TX FAULT ASSERTED, TX SIGNAL NOT RECOVERED



t-reset: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL RECOVERED



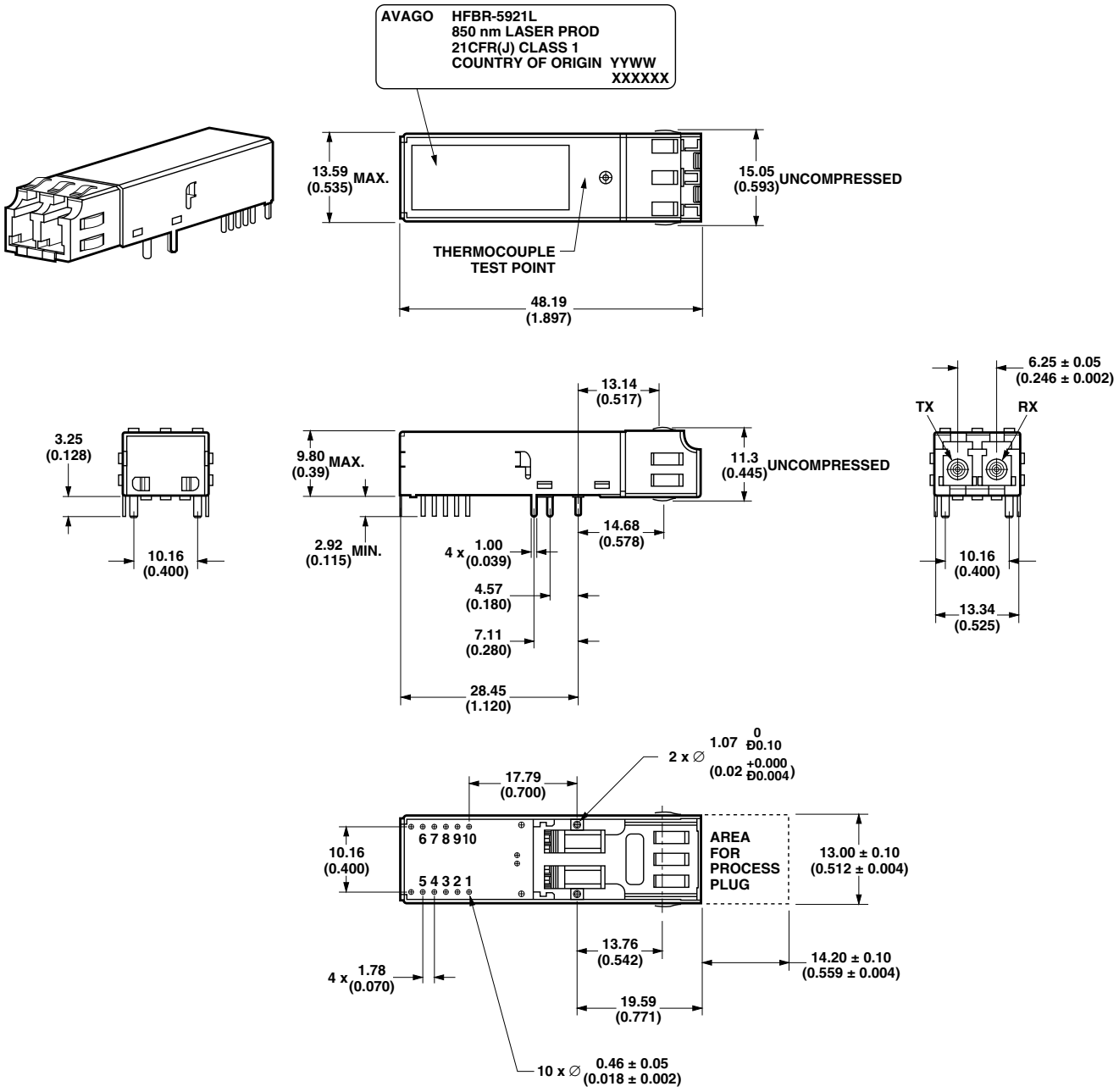
t-fault (2 x 6 only): TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL NOT RECOVERED



t-loss-on & t-loss-off

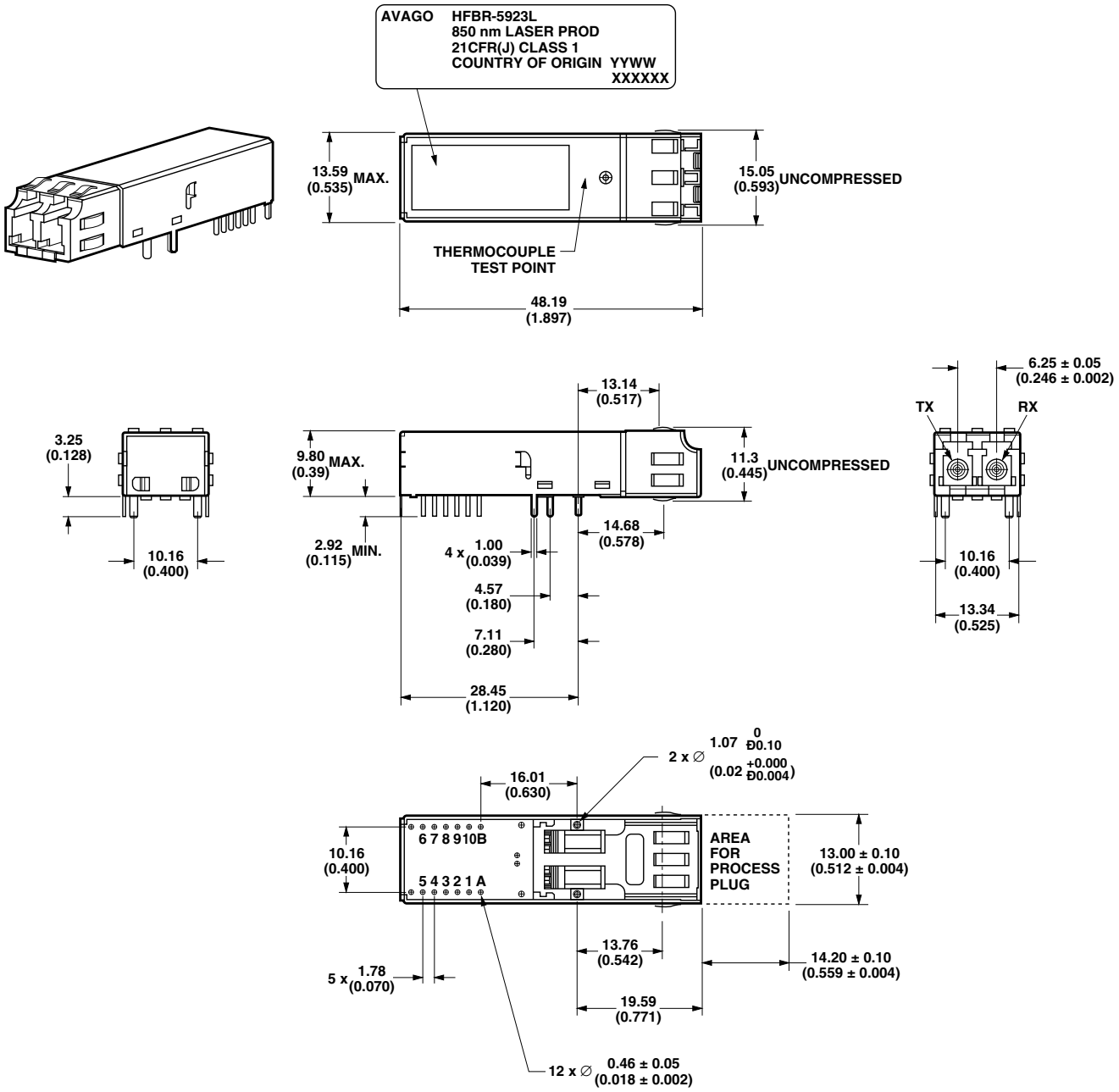
NOTE: Tx_FAULT IS AVAILABLE ONLY ON THE 2 x 6 OPTION – HFBR-5923L.

Figure 6. Transceiver timing diagrams.



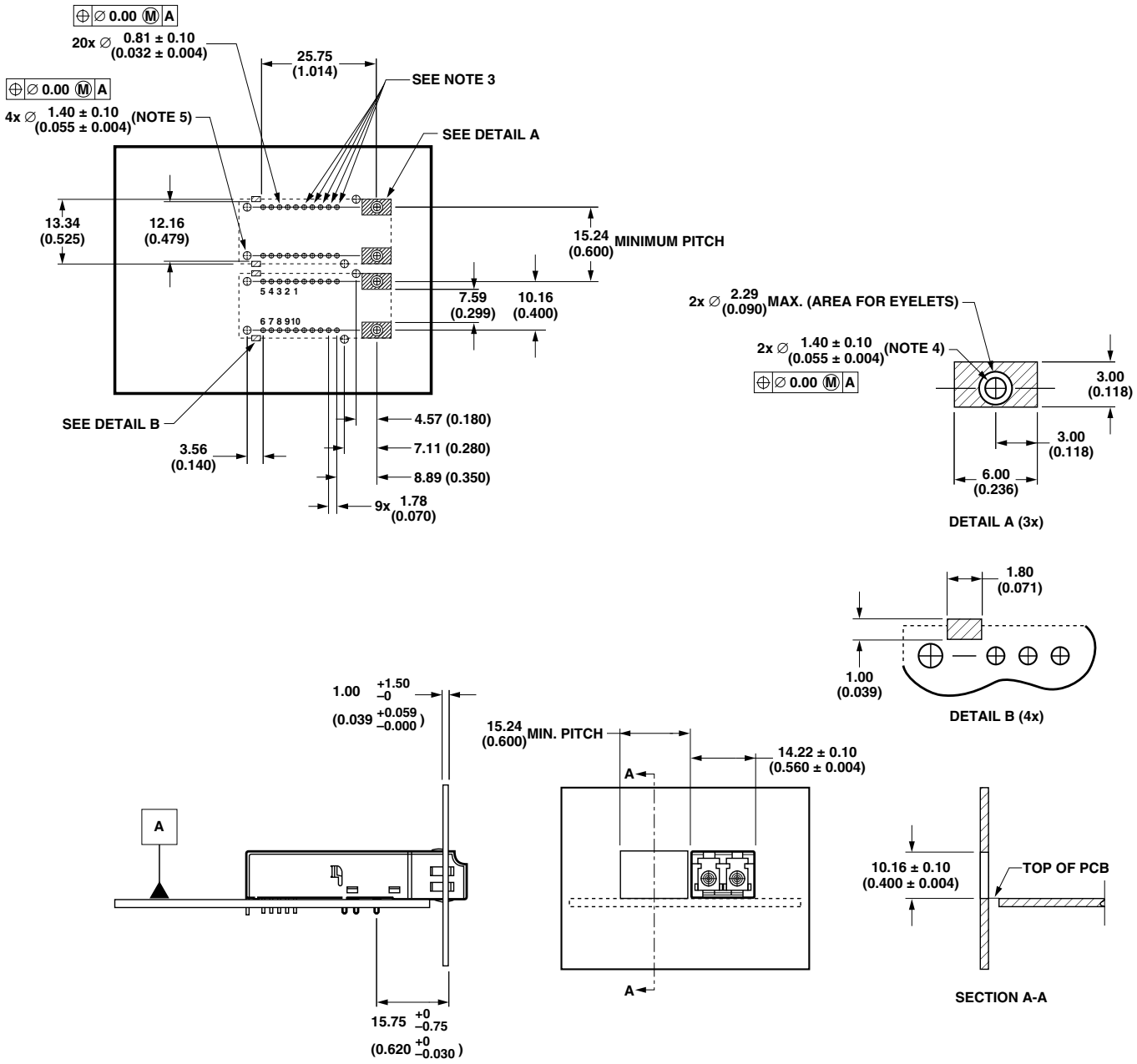
DIMENSIONS ARE IN MILLIMETERS (INCHES)

Figure 7a. 2 x 5 pin module drawing.



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Figure 7b. 2 x 6 pin module drawing.



NOTES

1. THIS PAGE DESCRIBES THE RECOMMENDED CIRCUIT BOARD LAYOUT AND FRONT PANEL OPENINGS FOR SFF TRANSCEIVERS.

2. THE HATCHED AREAS ARE KEEP-OUT AREAS RESERVED FOR HOUSING STANDOFFS. NO METAL TRACES ALLOWED IN KEEP-OUT AREAS.

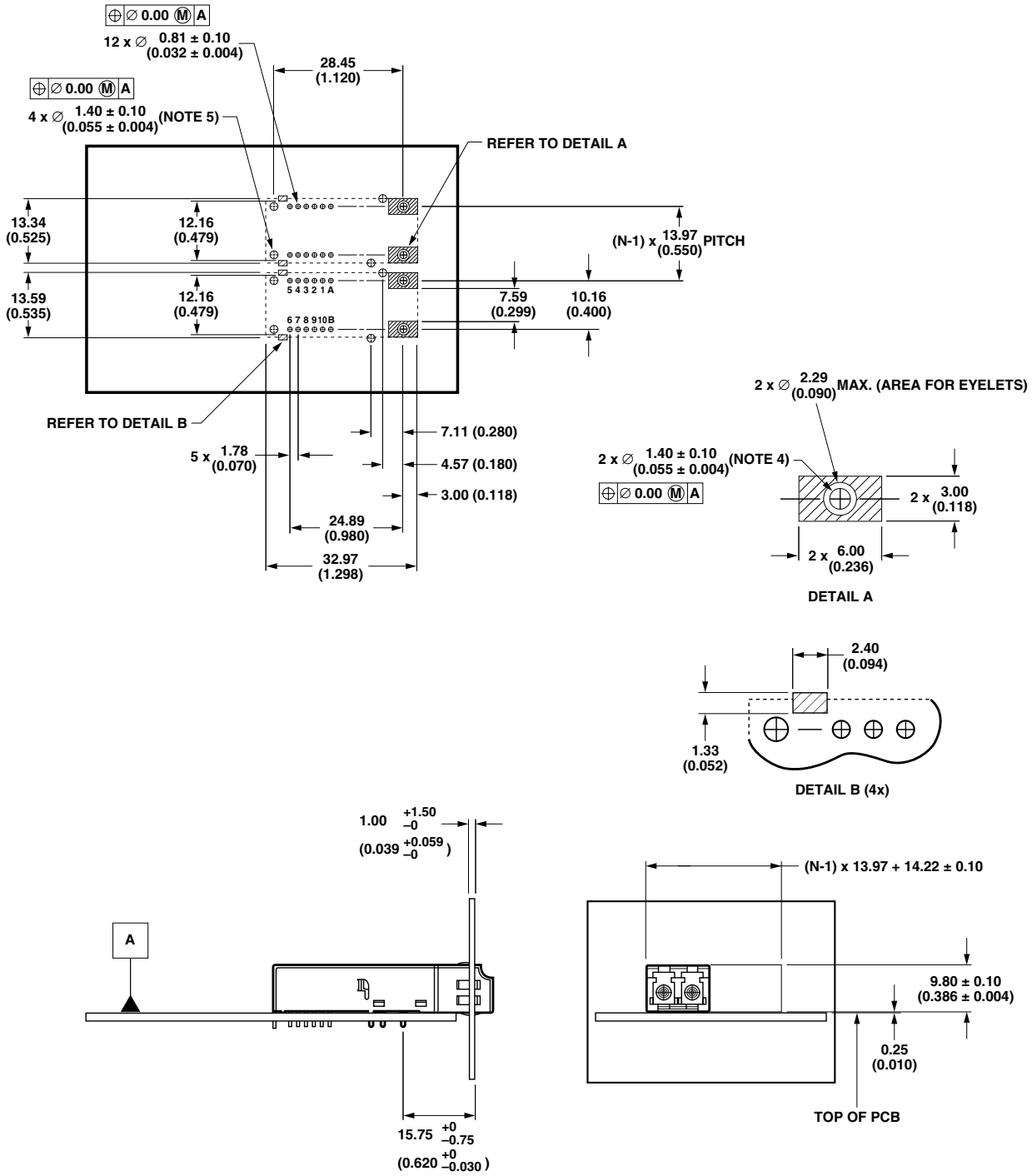
3. THE BOARD FOR 2 x 6 PIN TRANSCEIVERS IS SHOWN. THE BOARD FOR 2 x 5 PIN TRANSCEIVERS LACKS HOLES FOR PIN A AND PIN B.

4. HOLES FOR MOUNTING STUDS MUST BE TIED TO CHASSIS GROUND.

5. HOLES FOR HOUSING LEADS MUST BE TIED TO SIGNAL GROUND.

6. DIMENSIONS ARE IN MILLIMETERS (INCHES).

Figure 7c. Recommended SFF host board and front panel layout.



NOTES

1. THIS PAGE DESCRIBES AN ALTERNATE CIRCUIT BOARD LAYOUT AND FRONT PANEL OPENING FOR SFF TRANSCIEVERS. THE TRANSCEIVERS' PITCH IS CLOSER, AND ALL TRANSCEIVERS SHARE ONE COMMON OPENING IN THE FRONT PANEL.
2. THE HATCHED AREAS ARE KEEP-OUT AREAS RESERVED FOR HOUSING STANDOFFS. NO METAL TRACES ALLOWED IN KEEP-OUT AREAS.
3. THE BOARD FOR 2 x 6 PIN TRANSCEIVERS IS SHOWN. THE BOARD FOR 2 x 5 PIN TRANSCEIVERS LACKS HOLES FOR PIN A AND PIN B.
4. HOLES FOR MOUNTING STUDS MUST BE TIED TO CHASSIS GROUND.
5. HOLES FOR HOUSING LEADS MUST BE TIED TO SIGNAL GROUND.
6. N IS THE NUMBER OF TRANSCEIVERS MOUNTED ON THE PCB.
7. DIMENSIONS ARE IN MILLIMETERS (INCHES)

Figure 7d. Alternate SFF host board and front panel layout (for closer pitch).

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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