



### Features

- 10-bit Resolution
- 20/40 MSPS Maximum Sampling Rate
- Ultra-Low Power Dissipation: 24/43 mW
- 61.6 dB SNR @ 8 MHz
- Internal Reference Circuitry
- 1.8 V Core Supply Voltage
- 1.7 – 3.6 V I/O Supply Voltage
- Parallel CMOS Output
- 9 x 9 mm 64-Pin QFN (LP9E) Package
- Dual Channel

### Typical Applications

- Medical Imaging
- Portable Test Equipment
- Digital Oscilloscopes
- IF Communication

### Functional Diagram

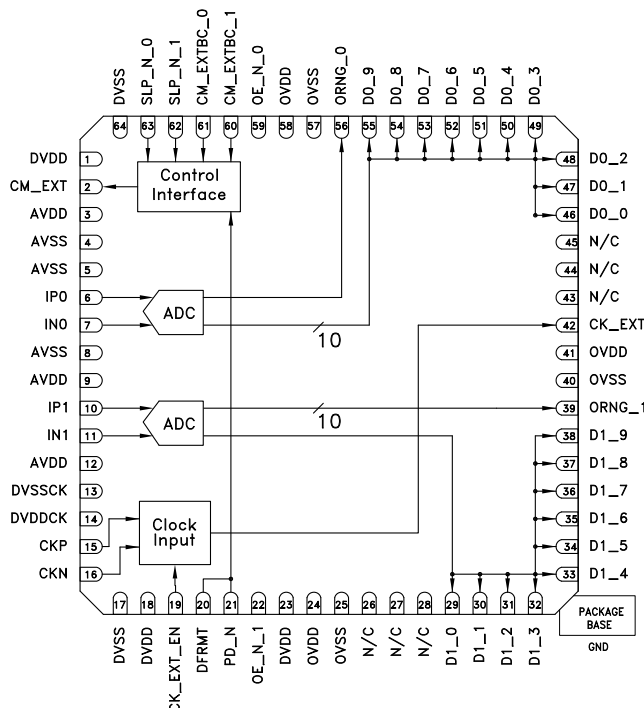


Figure 1. Functional Block Diagram

### General Description

The HMCAD1040-40 is a high performance low power dual analog-to-digital converter (ADC). The ADC employs internal reference circuitry, a CMOS control interface, CMOS output data and is based on a proprietary structure. Digital error correction is employed to ensure no missing codes in the complete full scale range.

Several idle modes with fast startup times exist. Each channel can be independently powered down and the entire chip can either be put in Standby Mode or Power Down mode. The different modes are optimized to allow the user to select the mode resulting in the lowest possible energy consumption during idle mode and startup.

The HMCAD1040-40 has a highly linear THA optimized for frequencies up to Nyquist. The differential clock interface is optimized for low jitter clock sources and supports LVDS, LVPECL, sine wave and CMOS clock inputs.

Pin compatible with HMCAD1040-80, HMCAD1050-40 and HMCAD1050-80.



**Electrical Specifications**

**DC Electrical Specifications**

AVDD= 1.8V, DVDD= 1.8V, DVDDCK= 1.8V, OVDD= 2.5V, 20/40 MSPS clock, 50% clock duty cycle, -1 dBFS 8 MHz input signal, unless otherwise noted

Parameter	Condition	Min.	Typ.	Max.	Units
<b>DC Accuracy</b>					
No missing codes		Guaranteed			
Offset error	Mid-scale offset		1		LSB
Gain error	Full scale range deviation from typical			± 6	%FS
Gain matching	Gain matching between channels. ± 3 sigma value at worst case conditions		± 0.5		%FS
DNL	Differential nonlinearity		± 0.15		LSB
INL	Integral nonlinearity		± 0.2		LSB
VCM	Common mode voltage output		VAVDD/2		V
<b>Analog Input</b>					
Input common mode	Analog input common mode voltage	VCM -0.1		VCM +0.2	V
Full scale range	Differential input voltage range		2.0		V <sub>pp</sub>
Input capacitance	Differential input capacitance		2		pF
Bandwidth	Input Bandwidth	500			MHz
<b>Power Supply</b>					
Core Supply Voltage	Supply voltage to all 1.8V domain pins. See Pin Configuration and Description	1.7	1.8	2.0	V
I/O Supply Voltage	Output driver supply voltage (OVDD). Should be higher than or equal to Core Supply Voltage (VOVDD ≥ VD VDD)	1.7	2.5	3.6	V

**AC Electrical Specifications - 20 MSPS**

AVDD= 1.8V, DVDD= 1.8V, DVDDCK= 1.8V, OVDD= 2.5V, FS= 20 MSPS clock, 50% clock duty cycle, -1 dBFS 8 MHz input signal, unless otherwise noted.

Parameter	Condition	Min.	Typ.	Max.	Units
<b>Performance</b>					
SNR	Signal to Noise Ratio				
	FIN = 2 MHz		61.7		dBFS
	FIN = 8 MHz	60	61.6		dBFS
	FIN =- FS/2		61.6		dBFS
SNDR	Signal to Noise and Distortion Ratio				
	FIN = 2 MHz		61.7		dBFS
	FIN = 8 MHz	60	61.6		dBFS
	FIN =- FS/2		60.5		dBFS
SFDR	Spurious Free Dynamic Range				
	FIN = 2 MHz		80		dBc
	FIN = 8 MHz	70	81		dBc
	FIN =- FS/2		70		dBc
HD2	Second order Harmonic Distortion				
	FIN = 2 MHz		-90		dBc
	FIN = 8 MHz	-80	-90		dBc
	FIN =- FS/2		-90		dBc
HD3	Third order Harmonic Distortion				
	FIN = 2 MHz		-80		dBc
	FIN = 8 MHz	-70	-81		dBc
	FIN =- FS/2		-70		dBc
ENOB	Effective number of Bits				
	FIN = 2 MHz		10.0		bits
	FIN = 8 MHz	9.7	9.9		bits
	FIN =- FS/2		9.8		bits
Crosstalk	Signal crosstalk between channels, FIN1=8MHz, FIN0=9.9MHz				
			-105		dB
<b>Power Supply</b>					
Analog supply current			8.2		mA
Digital supply current	Digital core supply				
			1.7		mA
Output driver supply	2.5V output driver supply, sine wave input, FIN = 1 MHz, CK_EXT enabled				
			2.8		mA
Output driver supply	2.5V output driver supply, sine wave input, FIN = 1 MHz, CK_EXT disabled				
			2.3		mA
Analog power Dissipation			14.8		mW
Digital power Dissipation	OVDD = 2.5V, 5pF load on output bits, FIN = 1 MHz, CK_EXT disabled				
			8.8		mW
Total power Dissipation	OVDD = 2.5V, 5pF load on output bits, FIN = 1 MHz, CK_EXT disabled				
			23.6		mW
Power Down Dissipation			9.9		mW
Sleep Mode 1	Power Dissipation, Sleep mode one channel				
			15.2		mW
Sleep Mode 2	Power Dissipation, Sleep mode both channels				
			7.7		mW
<b>Clock Inputs</b>					
Max. Conversion Rate		20			MSPS
Min. Conversion Rate				3	MSPS

**AC Electrical Specifications - 40 MSPS**

AVDD= 1.8V, DVDD= 1.8V, DVDDCK= 1.8V, OVDD= 2.5V, FS= 40 MSPS clock, 50% clock duty cycle, -1 dBFS 8 MHz input signal, unless otherwise noted.

Parameter	Condition	Min.	Typ.	Max.	Units
<b>Performance</b>					
SNR	Signal to Noise Ratio				
	FIN = 2 MHz		61.6		dBFS
	FIN = 8 MHz	60	61.6		dBFS
	FIN = FS/2		61.6		dBFS
SNDR	Signal to Noise and Distortion Ratio				
	FIN = 2 MHz		61.6		dBFS
	FIN = 8 MHz	60	61.6		dBFS
	FIN = FS/2		61.2		dBFS
SFDR	Spurious Free Dynamic Range				
	FIN = 2 MHz		80		dBc
	FIN = 8 MHz	70	81		dBc
	FIN = FS/2		72		dBc
HD2	Second order Harmonic Distortion				
	FIN = 2 MHz		-90		dBc
	FIN = 8 MHz	-80	-90		dBc
	FIN = FS/2		-85		dBc
HD3	Third order Harmonic Distortion				
	FIN = 2 MHz		-80		dBc
	FIN = 8 MHz	-70	-81		dBc
	FIN = FS/2		-72		dBc
ENOB	Effective number of Bits				
	FIN = 2 MHz		9.9		bits
	FIN = 8 MHz	9.7	9.9		bits
	FIN = FS/2		9.8		bits
Crosstalk	Signal crosstalk between channels, FIN1 = 8 MHz, FIN0 = 9.9 MHz				
			-100		dB
<b>Power Supply</b>					
Analog supply current			14.4		mA
Digital supply current	Digital core supply		3.4		mA
Output driver supply	2.5V output driver supply, sine wave input, FIN = 1 MHz, CK_EXT enabled		5.1		mA
Output driver supply	2.5V output driver supply, sine wave input, FIN = 1 MHz, CK_EXT disabled		4.2		mA
Analog power Dissipation			25.9		mW
Digital power Dissipation	OVDD = 2.5V, 5pF load on output bits, FIN = 1 MHz, CK_EXT disabled		16.6		mW
Total power Dissipation	OVDD = 2.5V, 5pF load on output bits, FIN = 1 MHz, CK_EXT disabled		42.5		mW
Power Down Dissipation			9.7		mW
Sleep Mode 1	Power Dissipation, Sleep mode one channel		25.7		mW
Sleep Mode 2	Power Dissipation, Sleep mode both channels		11.3		mW
<b>Clock Inputs</b>					
Max. Conversion Rate		40			MSPS
Min. Conversion Rate				3	MSPS

## Digital & Timing Specifications

AVDD= 1.8V, DVDD= 1.8V, DVDDCK= 1.8V, OVDD= 2.5V, Conversion Rate: Max specified, 50% clock duty cycle, -1dBFS input signal, 5 pF capacitive load on data outputs, unless otherwise noted

Parameter	Condition	Min	Typ	Max	Unit
<b>Clock Inputs</b>					
Duty Cycle		20		80	% high
Compliance		CMOS, LVDS, LVPECL, Sine Wave			
Input range	Differential input swing	0.4			V <sub>pp</sub>
Input range	Differential input swing, sine wave clock input	1.6			V <sub>pp</sub>
Input common mode voltage	Keep voltages within ground and voltage of OVDD	0.3		V <sub>OVDD</sub> -0.3	V
Input capacitance	Differential		2		pF
<b>Timing</b>					
T <sub>PD</sub>	Start up time from Power Down Mode to Active Mode			900	clock cycles
T <sub>SLP</sub>	Start up time from Sleep Mode to Active Mode			20	clock cycles
T <sub>OVR</sub>	Out of range recovery time		1		clock cycles
T <sub>AP</sub>	Aperture Delay		0.8		ns
Crms	Aperture jitter		< 0.5		ps
T <sub>LAT</sub>	Pipeline Delay		12		clock cycles
T <sub>D</sub>	Output delay (see timing diagram). 5pF load on output bits	3		10	ns
T <sub>DC</sub>	Output delay relative to CK_EXT (see timing diagram)	1		6	ns
<b>Logic Inputs</b>					
V <sub>HI</sub>	High Level Input Voltage. V <sub>OVDD</sub> ≥ 3.0V	2			V
V <sub>HI</sub>	High Level Input Voltage. V <sub>OVDD</sub> = 1.7V – 3.0V	0.8 · V <sub>OVDD</sub>			V
V <sub>LI</sub>	Low Level Input Voltage. V <sub>OVDD</sub> ≥ 3.0V	0		0.8	V
V <sub>LI</sub>	Low Level Input Voltage. V <sub>OVDD</sub> = 1.7V – 3.0V	0		0.2 · V <sub>OVDD</sub>	V
I <sub>HI</sub>	High Level Input leakage Current			±10	μA
I <sub>LI</sub>	Low Level Input leakage Current			±10	μA
C <sub>I</sub>	Input Capacitance		3		pF
<b>Logic Outputs</b>					
V <sub>HO</sub>	High Level Output Voltage		V <sub>OVDD</sub> -0.1		V
V <sub>LO</sub>	Low Level Output Voltage			0.1	V
C <sub>L</sub>	Max capacitive load. Post-driver supply voltage equal to pre-driver supply voltage V <sub>OVDD</sub> = V <sub>OCVDD</sub>			5	pF
C <sub>L</sub>	Max capacitive load. Post-driver supply voltage above 2.25V <sup>[1]</sup>		10		pF

[1] The outputs will be functional with higher loads. However, it is recommended to keep the load on output data bits as low as possible to keep dynamic currents and resulting switching noise at a minimum

### Timing Diagram

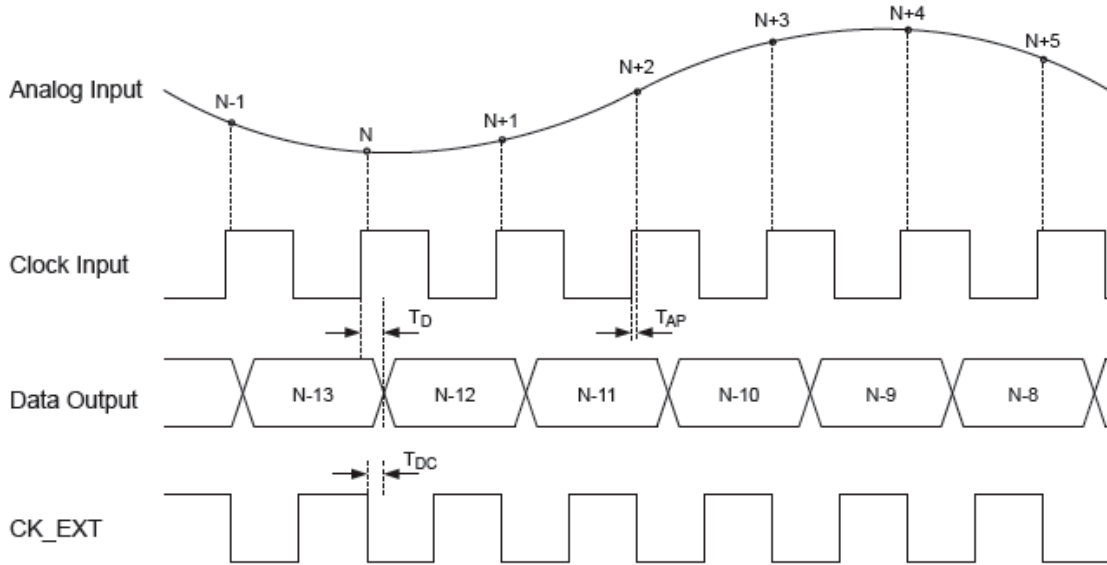


Figure 2. Timing Diagram

**Table 1. Absolute Maximum Ratings**

Pin	Pin	Pin
AVDD	AVSS	-0.3V to +2.3V
DVDD	DVSS	-0.3V to +2.3V
AVSS, DVSSCK, DVSS, OVSS	DVSS	-0.3V to +0.3V
OVDD	OVSS	-0.3V to +3.9V
IPx, INx, analog inputs and outputs	AVSS	-0.3V to +2.3V
Digital outputs	OVSS	-0.3V to +3.9V
CKP, CKN	DVSSCK	-0.3V to +3.9V
Digital Inputs	OVSS	-0.3V to +3.9V
Operating temperature		-40 to +85 °C
Storage temperature		-60 to +150 °C
Soldering Profile Qualification		J-STD-020



**ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

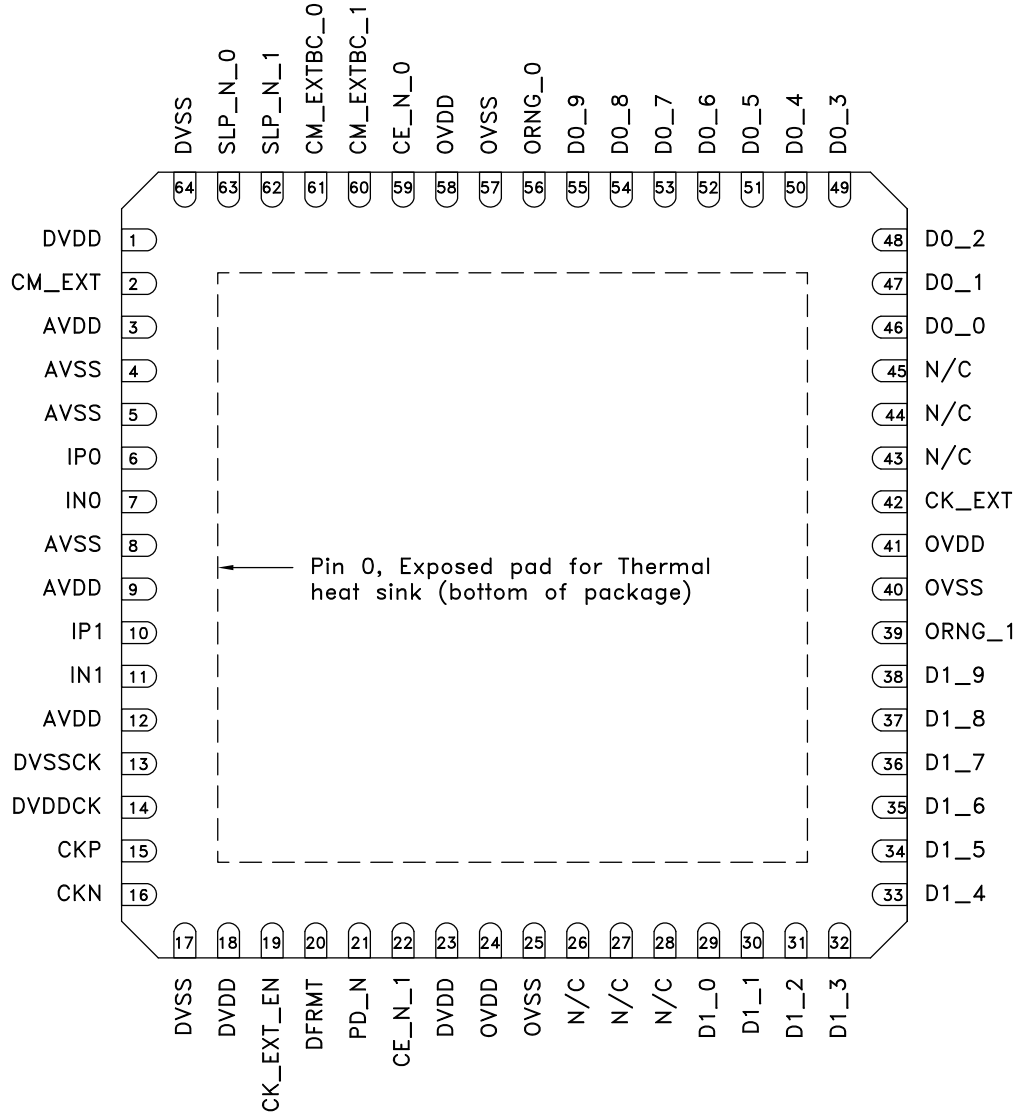
**Pin Configuration and Description**


Figure 3. Package Drawing, QFN 64-Pin

**Table 2. Pin Descriptions**

Pin Number	Function	Description
1, 18, 23	DVDD	Digital and I/O-ring pre driver supply voltage, 1.8V
2	CM_EXT	Common Mode voltage output
3, 9, 12	AVDD	Analog supply voltage, 1.8V
4, 5, 8	AVSS	Analog ground
6, 7	IP0, IN0	Analog input Channel 0 (non-inverting, inverting)
10, 11	IP1, IN1	Analog input Channel 1 (non-inverting, inverting)
13	DVSSCK	Clock circuitry ground
14	DVDDCK	Clock circuitry supply voltage, 1.8V
15	CKP	Clock input, non-inverting (Format: LVDS, LVPECL, CMOS/TTL, Sine Wave)
16	CKN	Clock input, inverting. For CMOS input on CKP, connect CKN to ground.
17, 64	DVSS	Digital circuitry ground
19	CK_EXT_EN	CK_EXT signal enabled when low (zero). Tristate when high.
20	DFRMT	Data format selection. 0: Offset Binary, 1: Two's Complement
21	PD_N	Full chip Power Down mode when Low. All digital outputs reset to zero. <b>After chip power up always apply Power Down mode before using Active Mode to reset chip.</b>
22	OE_N_1	Output Enable Channel 0. Tristate when high
24, 41, 58	OVDD	I/O ring post-driver supply voltage. Voltage range 1.7 to 3.6V
25, 40, 57	OVSS	Ground for I/O ring
26	NC	
27	NC	
28	NC	
29	D1_0	Output Data Channel 1 (LSB)
30	D1_1	Output Data Channel 1
31	D1_2	Output Data Channel 1
32	D1_3	Output Data Channel 1
33	D1_4	Output Data Channel 1
34	D1_5	Output Data Channel 1
35	D1_6	Output Data Channel 1
36	D1_7	Output Data Channel 1
37	D1_8	Output Data Channel 1
38	D1_9	Output Data Channel 1 (MSB)
39	ORNG_1	Out of Range flag Channel 1. High when input signal is out of range
42	CK_EXT	Output clock signal for data synchronization. CMOS levels
43	NC	
44	NC	
45	NC	
46	D0_0	Output Data Channel 0 (LSB)
47	D0_1	Output Data Channel 0
48	D0_2	Output Data Channel 0
49	D0_3	Output Data Channel 0




**Table 2. Pin Descriptions**

Pin Number	Function	Description
50	D0_4	Output Data Channel 0
51	D0_5	Output Data Channel 0
52	D0_6	Output Data Channel 0
53	D0_7	Output Data Channel 0
54	D0_8	Output Data Channel 0
55	D0_9	Output Data Channel 0 (MSB)
56	ORNG_0	Out of Range flag Channel 0. High when input signal is out of range
59	OE_N_0	Output Enable Channel 0. Tristate when high
60, 61	CM_EXTBC_1, CM_EXTBC_0	Bias control bits for the buffer driving pin CM_EXT 00: OFF                      01: 50uA 10: 500uA                    11: 1mA
62, 63	SLP_N_1, SLP_N_0	Sleep Mode 00: Sleep Mode              01: Channel 0 active 10: Channel 1 active        11: Both channels active

### Recommended Usage

#### Analog Input

The analog input to the HMCAD1040-40 is a switched capacitor track-and-hold amplifier optimized for differential operation. Operation at common mode voltages at mid supply is recommended even if performance will be good for the ranges specified. The CM\_EXT pin provides a voltage suitable as common mode voltage reference. The internal buffer for the CM\_EXT voltage can be switched off, and driving capabilities can be changed by using the CM\_EXTBC control input.

Figure 4 shows a simplified drawing of the input network. The signal source must have sufficiently low output impedance to charge the sampling capacitors within one clock cycle. A small external resistor (e.g. 22 Ohm) in series with each input is recommended as it helps reduce transient currents and dampens ringing behavior. A small differential shunt capacitor at the chip side of the resistors may be used to provide dynamic charging currents and may improve performance. The resistors form a low pass filter with the capacitor, and values must therefore be determined by requirements for the application.

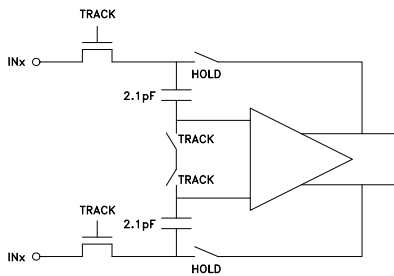


Figure 4. Input configuration

#### DC-Coupling

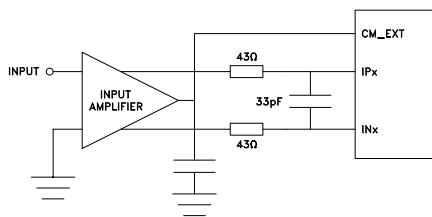


Figure 5. DC coupled input with buffer

Figure 5 shows a recommended configuration for DC-coupling. Note that the common mode input voltage must be controlled according to specified values.

Preferably, the CM\_EXT output should be used as reference to set the common mode voltage.

The input amplifier could be inside a companion chip or it could be a dedicated amplifier. Several suitable single ended to differential driver amplifiers exist in the market. The system designer should make sure the specifications of the selected amplifier is adequate for the total system, and that driving capabilities comply with the HMCAD1040-40 input specifications.

Detailed configuration and usage instructions should be found in the documentation of the selected driver, and the values given in figure 5 must be varied according to the recommendations for the driver.

#### AC-Coupling

A signal transformer or series capacitors can be used to make an AC-coupled input network. Figure 6 shows a recommended configuration using a transformer. Make sure that a transformer with sufficient linearity is selected, and that the bandwidth of the transformer is appropriate. The bandwidth should exceed the sampling rate of the ADC with at least a factor of 10. It is also important to minimize phase mismatch between the differential ADC inputs for good HD2 performance. This type of transformer coupled input is the preferred configuration for high frequency signals as most differential amplifiers do not have adequate performance at high frequencies. Magnetic coupling between the transformers and PCB traces may impact channel crosstalk, and must be taken into account during PCB layout. If the input signal is traveling a long physical distance from the signal source to the transformer (for example a long cable), kick-backs from the ADC will also travel along this distance. If these kick-backs are not terminated properly at the source side, they are reflected and will add to the input signal at the ADC input. This could reduce the ADC performance. To avoid this effect, the source must effectively terminate the ADC kick-backs, or the traveling distance should be very short. If this problem could not be avoided, the circuit in figure 8 can be used.

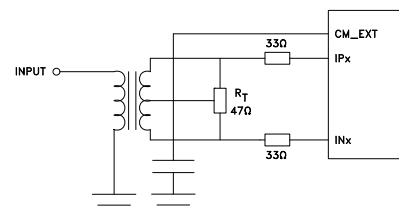


Figure 6. Transformer coupled input

Figure 7 shows AC-coupling using capacitors. Resistors from the CM\_EXT output, R<sub>CM</sub>, should be used to bias the differential input signals to the correct voltage. The series capacitor, C<sub>I</sub>, form the high-pass pole with these resistors, and the values must therefore be determined based on the requirement to the high-pass cut-off frequency.

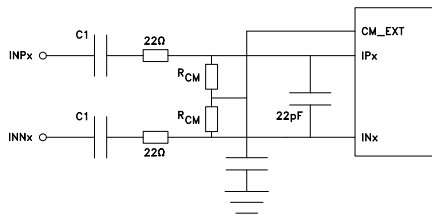


Figure 7. AC coupled input

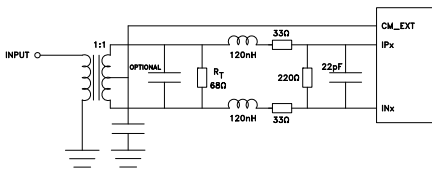


Figure 8. Alternative input network

Note that startup time from Sleep Mode and Power Down Mode will be affected by this filter as the time required to charge the series capacitors is dependent on the filter cut-off frequency.

If the input signal has a long traveling distance, and the kick-backs from the ADC not are effectively terminated at the signal source, the input network of figure 8 can be used. The configuration in figure 8 is designed to attenuate the kickback from the ADC and to provide an input impedance that looks as resistive as possible for frequencies below Nyquist. Values of the series inductor will however depend on board design and conversion rate. In some instances a shunt capacitor in parallel with the termination resistor (e.g. 33 pF) may improve ADC performance further. This capacitor attenuates the ADC kick-back even more, and minimizes the kicks traveling towards the source. However, the impedance match seen into the transformer becomes worse.

### Clock Input and Jitter considerations

Typically high-speed ADCs use both clock edges to generate internal timing signals. In the HMCAD1040-40 only the rising edge of the clock is used. Hence, input clock duty cycles between 20% and 80% are acceptable.

The input clock can be supplied in a variety of formats. The clock pins are AC-coupled internally. Hence a wide common mode voltage range is accepted. Differential clock sources as LVDS, LVPECL or differential sine wave can be connected directly to the input pins. For CMOS inputs, the CKN pin should be connected to ground, and the CMOS clock signal should be connected to CKP. For differential sine wave clock, the input amplitude must be at least  $\pm 800$  mVpp.

The quality of the input clock is extremely important for high-speed, high-resolution ADCs. The contribution to SNR from clock jitter with a full scale signal at a given frequency is shown in equation 1,

$$SNR_{jitter} = 20 \cdot \log(2 \cdot \pi \cdot f_{IN} \cdot \epsilon_t) \quad (1)$$

where  $f_{IN}$  is the signal frequency, and  $\epsilon_t$  is the total rms jitter measured in seconds. The rms jitter is the total of all jitter sources including the clock generation circuitry, clock distribution and internal ADC circuitry.

For applications where jitter may limit the obtainable performance, it is of utmost importance to limit the clock jitter. This can be obtained by using precise and stable clock references (e.g. crystal oscillators with good jitter specifications) and make sure the clock distribution is well controlled. It might be advantageous to use analog power and ground planes to ensure low noise on the supplies to all circuitry in the clock distribution. It is of utmost importance to avoid crosstalk between the ADC output bits and the clock and between the analog input signal and the clock since such crosstalk often results in harmonic distortion.

The jitter performance is improved with reduced rise and fall times of the input clock. Hence, optimum jitter performance is obtained with LVDS or LVPECL clock with fast edges. CMOS and sine wave clock inputs will result in slightly degraded jitter performance.

If the clock is generated by other circuitry, it should be re-timed with a low jitter master clock as the last operation before it is applied to the ADC clock input.

### Digital Outputs

Digital output data are presented in parallel CMOS form. The voltage on the OVDD pin sets the levels of the CMOS outputs. The output drivers are dimensioned to drive a wide range of loads for OVDD above 2.25V, but it is recommended to minimize the load to ensure as low transient switching currents and resulting noise as possible. In applications with a large fanout or large



capacitive loads, it is recommended to add external buffers located close to the ADC chip.

The timing is described in the Timing Diagram section. Note that the load or equivalent delay on CK\_EXT always should be lower than the load on data outputs to ensure sufficient timing margins.

The digital outputs can be set in tristate mode by setting the OE\_N signal high.

The HMCAD1040-40 employs digital offset correction. This means that the output code will be 4096 with shorted inputs. However, small mismatches in parasitics at the input can cause this to alter slightly. The offset correction also results in possible loss of

codes at the edges of the full scale range. With no offset correction, the ADC would clip in one end before the other, in practice resulting in code loss at the opposite end. With the output being centered digitally, the output will clip, and the out of range flags will be set, before max code is reached. When out of range flags are set, the code is forced to all ones for overrange and all zeros for underrange.

### Data Format Selection

The output data are presented on offset binary form when DFRMT is low (connected to OVSS). Setting DFRMT high (connected to OVDD) results in 2's complement output format. Details are shown in table 3.

**Table 3: Data Format Description for 2Vpp full scale range**

Differential Input Voltage (IPx - INx)	Output data: Dx_9 : Dx_0 (DFRMT = 0, offset binary)	Output Data: Dx_9 : Dx_0 (DFRMT = 1, 2's complement)
1.0 V	11 1111 1111	01 1111 1111
+0.24mV	10 0000 0000	00 0000 0000
-0.24mV	01 1111 1111	11 1111 1111
-1.0V	00 0000 0000	10 0000 0000

### Reference Voltages

The reference voltages are internally generated and buffered based on a bandgap voltage reference. No external decoupling is necessary, and the reference voltages are not available externally. This simplifies usage of the ADC since two extremely sensitive pins, otherwise needed, are removed from the interface.

### Operational Modes

The operational modes are controlled with the PD\_N and SLP\_N pins. If PD\_N is set low, all other control pins are overridden and the chip is set in Power Down mode. In this mode all circuitry is completely turned off and the internal clock is disabled. Hence, only leakage current contributes to the Power Down Dissipation. The startup time from this mode is longer than for other idle modes as all references need to settle to their final values before normal operation can resume.

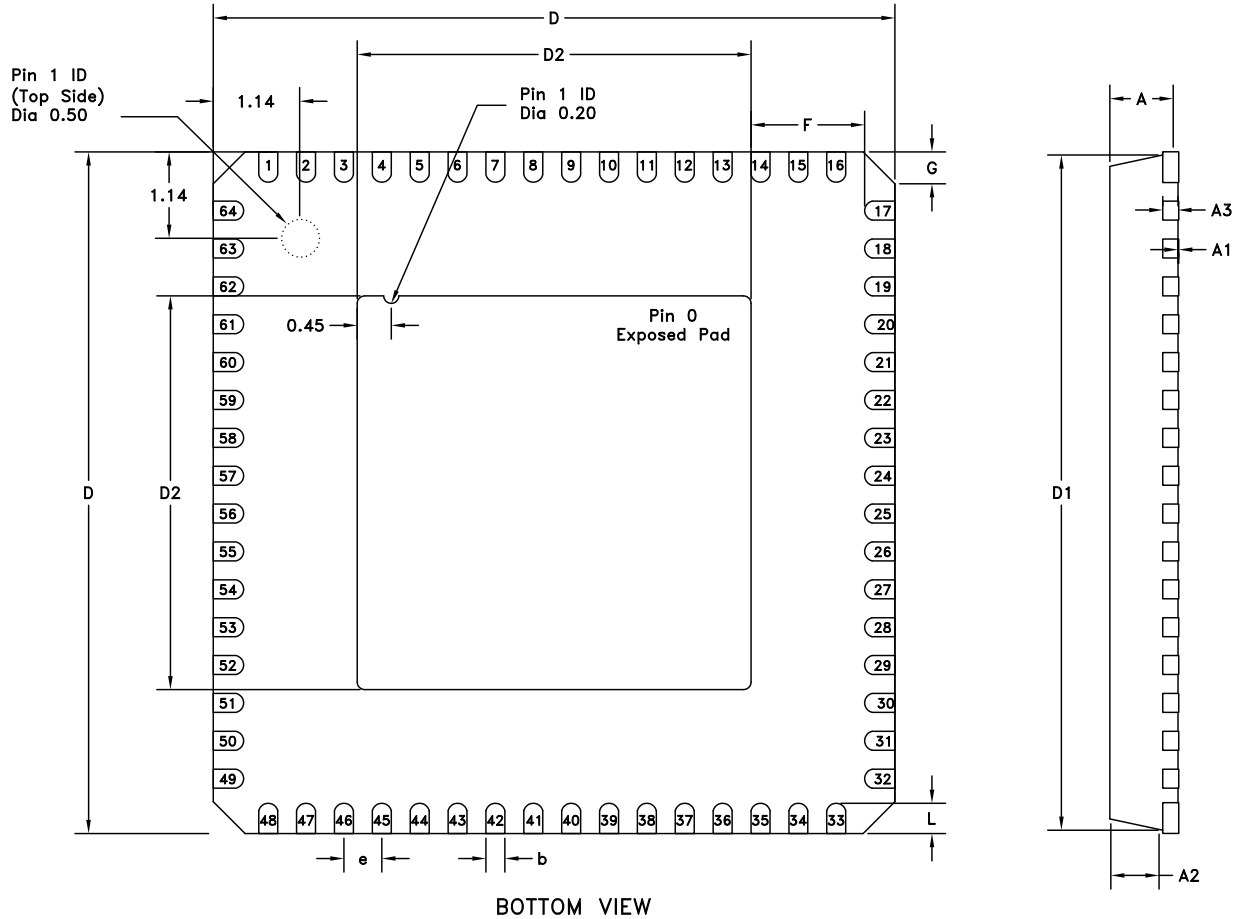
The SLP\_N bus can be used to power down each channel independently, or to set the full chip in Sleep Mode. In this mode internal clocking is disabled, but some low bandwidth circuitry is kept on to allow for a short startup time. However, Sleep Mode represents a significant reduction in supply current, and it can be used to save power even for short idle periods.

The input clock should be kept running in all idle modes. However, even lower power dissipation is possible in Power Down mode if the input clock is stopped. In this case it is important to start the input clock prior to enabling active mode.

### Startup Initialization

The HMCAD1040-40 must be reset prior to normal operation. This is required every time the power supply voltage has been switched off. A reset is performed by applying Power Down mode. Wait until a stable supply voltage has been reached, and pull the PD\_N pin for the duration of at least one clock cycle. The input clock must be running continuously during this Power Down period and until active operation is reached. Alternatively the PD pin can be kept low during power-up, and then be set high when the power supply voltage is stable.

### Outline Drawing



**Table 4. 9x9mm QFN (64 Pin LP9) Dimensions**

Symbol	Millimeter			Inch		
	Min	Typ	Max	Min	Typ	Max
A			0.9			0.035
A1	0	0.01	0.05	0	0.0004	0.002
A2		0.65	0.7		0.026	0.028
A3	0.2 REF			0.008 REF		
b	0.2	0.25	0.3	0.008	0.01	0.012
D	9.00 bsc			0.354 bsc		
D1	8.75 bsc			0.344 bsc		
D2	3.79	3.99	4.19	0.149	0.157	0.165
L	0.3	0.4	0.5	0.012	0.016	0.02
e	0.50 bsc			0.020 bsc		
Θ1	0°		12°	0°		12°
F	1.9			0.075		
G	0.24	0.42	0.6	0.0096	0.0168	0.024



### Package Information

Part Number	Package Body Material	Lead Finish	MSL [1]	Package Marking [2]
HMCAD1040-40	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	Level 2A	ASD0400 XXXX XXXX

[1] MSL, Peak Temp: The moisture sensitivity level rating classified according to the JEDEC industry standard and to peak solder temperature.

[2] Proprietary marking XXXX, 4-Digit lot number XXXX