

Enpirion EN5336QI 3A DCDC Converter w/Integrated Inductor Evaluation Board

Introduction

Congratulations! You are evaluating a complete power system on silicon:

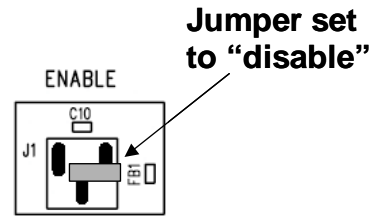
- The EN5336QI features integrated inductor, power MOSFETS, Gate Drive, Compensation Network, and controller and protection circuitry. This level of integration delivers a substantial reduction in footprint and part count over competing solutions.
- The EN5336QI features resistor divider output voltage programming. The resistor divider allows the user to set the output voltage to any value within the range 0.8V to $(V_{IN}-V_{DROPOUT})$. The evaluation board utilizes a small trim pot to adjust the output voltage. There is also a footprint for a fixed 0805 sized resistor to replace the trim pot.
- The user can also program the Over-Voltage-Protection (OVP) trip level using a separate resistor divider. The board does NOT come with the OVP resistors populated.
- The input capacitor is a 10V rated 22 μ F X5R MLCC. The output filter section is populated with 5 x 10 μ F 6.3V rated X5R MLC capacitors to achieve the required ~50 μ F of output capacitance. The combination of 5 x 10 μ F caps yields a very low ESR and hence low output ripple. A single 47 μ F capacitor can be substituted if a minimum footprint configuration is desired. The Soft-start capacitor is a small 10V rated 15nF X5R MLCC.
- Pads are available to add up to one additional input capacitor and there are a total of 5 pads to accommodate the output capacitor(s). This allows for evaluation of performance over a wide range of input/output capacitor combinations.
- Easy jumpers are provided for the following signals:
 - Enable
- Numerous test points are provided as well as banana plugs for input and output connections.
- The board comes with input decoupling and reverse polarity protection to protect the device from common setup mishaps.

Quick Start Guide

Figure 1 shows a top view of the evaluation board.

WARNING: complete steps 1 through 4 before applying power to the EN5336QI evaluation board.

STEP 1: Set the “ENABLE” jumper to the Disable Position.



STEP 2: Connect Power Supply to the input power connectors, VIN (+) and GND (-) as indicated in Figure 1.

CAUTION: be mindful of the polarity. Even though the evaluation board comes with reverse polarity protection diodes, it is rarely a good idea to reverse the input polarity.

STEP 3: Connect the load to the output connectors VOUT (+) and GND (-), as indicated in Figure 1.

STEP 4: Apply V_{IN} to the board and move the ENABLE jumper to the enabled position. The EN5336QI is now powered up!

NOTE: There is no de-bouncing circuitry associate with the enable pin.

NOTE: The trim pot is set at the factory to a predetermined output voltage. To adjust to another output voltage setting, turn the screw on the trim pot while monitoring the output voltage using an accurate volt-meter.

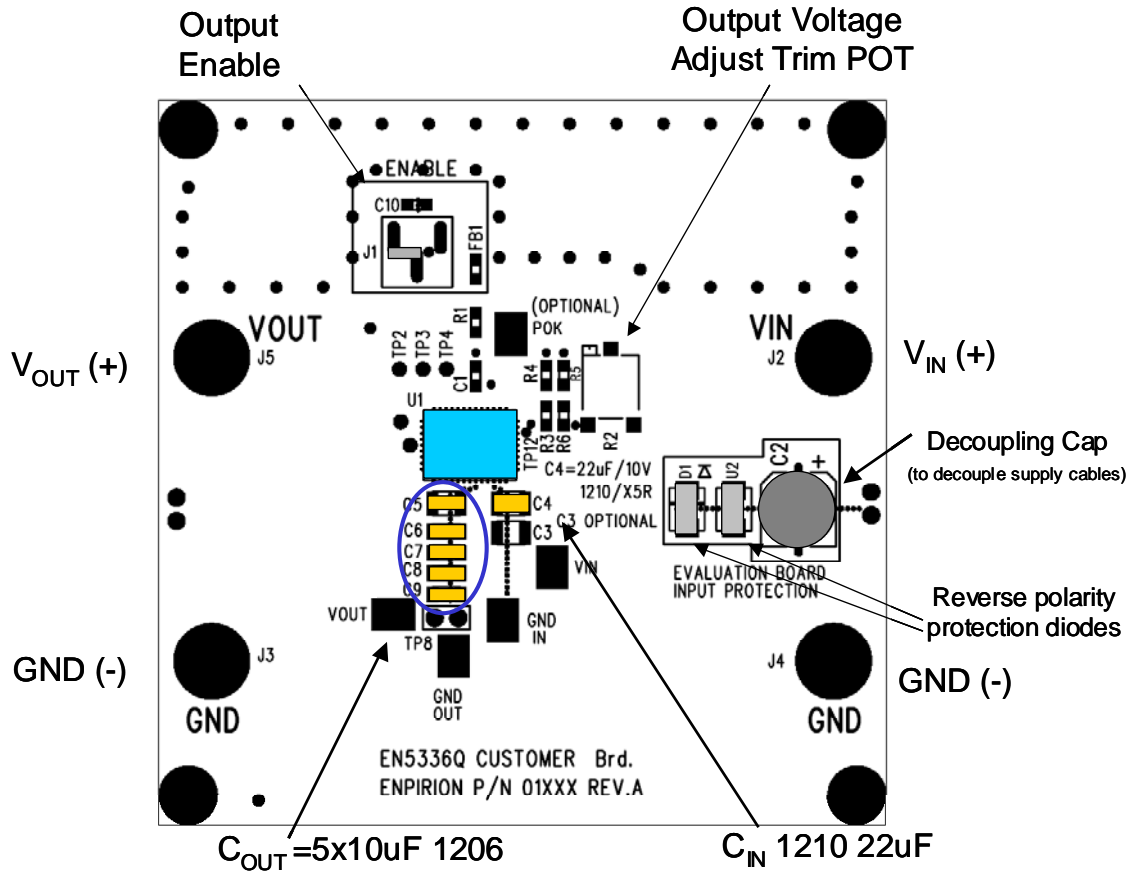


Figure 1. Evaluation Board Layout.

Output Voltage Select

Programming Output Voltage and OVP

The EN5336QI output voltage is programmed using a simple resistor divider network. Figure 2 shows a schematic view of the resistor divider configuration. The evaluation board uses a trim pot in place of resistor Ra1.

The EN5336QI output voltage and over voltage thresholds are determined by the voltages presented at the XFB and XOVP pins respectively. These voltages are set by way of resistor dividers between V_{OUT} and AGND with the midpoint going to XFB and XOVP.

It is recommended that Rb1 and Rb2 resistor values be $\sim 2k\Omega$. Use the following equation to set the resistor Ra1 for the desired output voltage:

$$Ra1 = \frac{(V_{out} - 0.75V) * Rb1}{0.75V}$$

If over-voltage protection is desired, use the following equation to set the resistor Ra2 for the desired OVP trip-point. Note that the evaluation board leaves these resistors un-populated.

$$Ra2 = \frac{(OVP_{trip} - 0.90V) * Rb2}{0.90V}$$

By design, if both resistor dividers are the same, the OV trip-point will be 20% above the nominal output voltage.

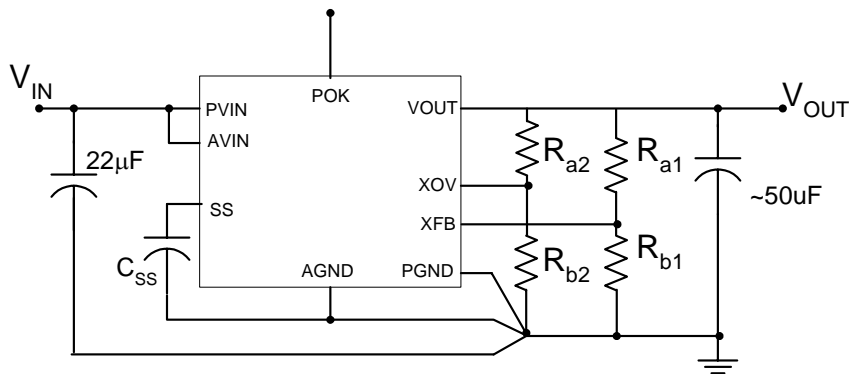


Figure 2. V_{OUT} and OVP resistor divider networks.

NOTE: if no OVP divider is present, there will be no over-voltage protection and POK will remain “high” as long as V_{OUT} remains above 90% of the nominal V_{OUT} setting.

Test Recommendations

To guarantee measurement accuracy, the following precautions should be observed:

1. Make all input and output voltage measurements at the board using the test points provided. This will eliminate voltage drop across the line and load cables that can produce false readings.
2. Measure input and output current with series ammeters or accurate shunt resistors. This is especially important when measuring efficiency.
3. Use a balanced impedance probe tip to measure switching signals to avoid noise coupling into the probe ground lead.

Input and Output Capacitors

The **input** capacitance requirement is 22uF for the EN5336QI. Enpirion recommends that a low ESR MLC capacitor be used. The voltage rating should be high enough to provide adequate margin for your application. There is a pre-tinned pad for one additional 1210 capacitor to experiment with input filter performance.

The **output** capacitance requirement is approximately 50uF of capacitance. The EN5336QI-E evaluation board comes populated with 5 x 10uF 6.3V 1206 MLC capacitors. The 5 parallel capacitors provide for reduced ESR and hence lower output ripple voltage. If a minimum footprint configuration is desired, the 5 x10uF capacitors can be replaced with a single 47uF MLC capacitor.

NOTE: Capacitors must be X5R or X7R dielectric formulations. Do not use Y5V dielectrics for input or output filter capacitors. Y5V capacitors lose capacitance with bias voltage, temperature, and frequency, and are not suitable for this application.

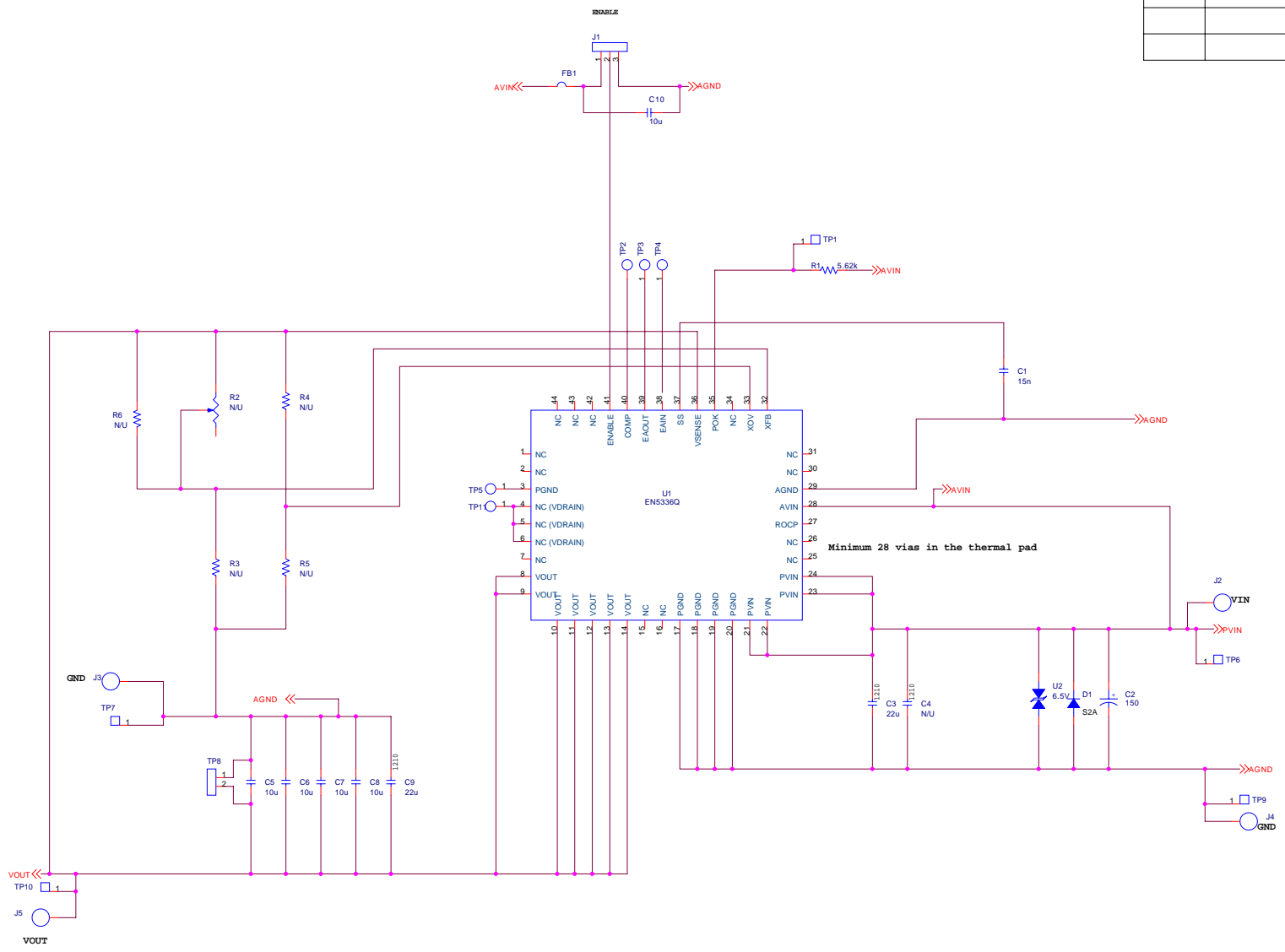
NOTE: Please refer to product datasheet for specific recommendations.

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Revision	Description	Date	Approved
p1	PRELIMINARY RELEASE	2/26/2006	CJR
p2	Added C10 and FB1	9/19/2006	CJR
p3	Removed PGND, Added TP5, TP11.	10/25/2006	CJR



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Title EN5336Q Customer Board			
Size	Drawing Number	Drawn By	Rev
		C. Romano	p3
Date	February 26, 2006	Sheet	1 of 1