S1D13L01

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S1D13L01 WQVGA Graphics Controller

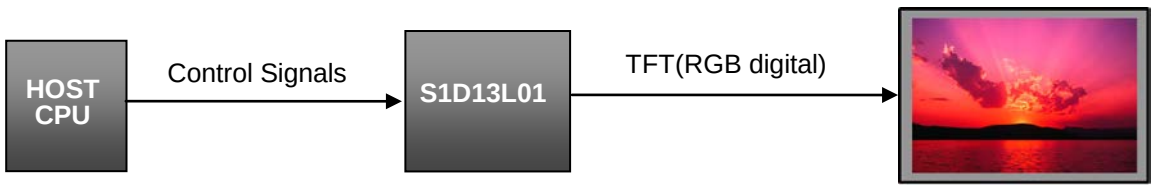
The S1D13L01 is a simple, multi-purpose Graphics LCD Controller with 384KByte embedded SRAM display buffer which supports both RGB interface TFT panels. The S1D13L01 supports most popular CPU interfaces in both 8/16-bit and Direct/Indirect variations. The embedded display buffer allows WQVGA up to 480x272 at 24bpp or 800x480 8bpp for single layer display, or 480x272 at 16bpp (Main Layer) and 480x272 at 8bpp (PIP Layer) for two layer display.

The S1D13L01's combination of multiple CPU interfaces and display interface types offers a versatile, yet easy to develop display system. Additionally, it offers Multiple Window support, Transparency and Alpha Blending functions. It is a flexible, low cost, low power, single chip solution designed to meet the demands of embedded markets such as low end IP phone devices where total system cost and battery life are major concerns. It's impartiality to CPU type or operating system also makes it an ideal display solution for a wide variety of other applications such as Office Automation, Medical instruments and Factory Automation applications.

■ FEATURES

- 384kByte Embedded Memory
- Direct and Indirect CPU Interfaces
- 8/16-bit data bus width
- SPI CPU interface
- Support for single panel implementation:
  - RGB Interface TFT panel
- Programmable resolutions (up to 800x480@8bpp) and color depth (up to 24 bpp)
- Multiple Window (Layer) support for Main and PIP
- Rotation (Swivel View) 90 /180 /270
- General Purpose IO Pins
- LUT 256wordx24bitx3pcs for both Main and PIP layer
- Alpha Blending, Transparency, Flashing
- Software initiated Power Save Mode
- H/PIOVDD: 3.3 or 1.8V, CORE/PLLVDD: 1.5V
- Clocks can be selected from embedded PLL or digital clock inputs
- Temperature Range: -40° ~ 85°
- Package: QFP15 128-pin, 0.4mm pin pitch

■ SYSTEM BLOCK DIAGRAM



S1D13L01 Features

Embedded display buffer
2 layer support
Alpha Blending and Transparency
PIP layer Flashing
Programmable PLL

■ DESCRIPTION

CPU Interface

- Support for most popular CPU interfaces
- Direct/Indirect Addressing
- 8/16-bit interface support
- SPI

Display Support

- Single panel implementation can be:
  - RGB Interface TFT panel
- Programmable resolutions up to 800x480@8bpp
- Programmable color depths up to 24 bpp

Display Features

- Multiple Window (Layer) support for Main and PIP
- Alpha Blending and Transparency
- PIP Flashing
- LUT 256wordx24bitx3pcs for both Main and PIP layer
- Rotation (Swivel View) 90 /180 /270

384KByte Embedded Memory

- Maximum Resolution for WQVGA:
  1 layer:
  480x272 at 24bpp or
  800x480 at 8bpp
  2 layer:
  Main 480x272 at 16bpp and
  PIP 480x272 at 8bpp

Miscellaneous

- Internal System Speed: 66MHz
- Software initiated power save mode
- Multiple General Purpose IO pins
- Flexible clock structure:
  - Embedded PLL
  - Digital clock inputs
- Operating Temperature Range: -40° ~ 85°
- Low Operating Voltage:
  PLL/CORE$_{VDD}$ 1.5 volts and
  PIO/HIO$_{VDD}$ 3.3 or 1.8 volts
- Package: QFP15 128-pin, 0.4mm pin pitch

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