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NTE2104
Integrated Circuit
4096 X 1 – Bit DYNAMIC RAM

Description:

The NTE2104 is a 4096 word by 1 bit MOS random access memory circuit fabricated with an N – Channel Silicon Gate Process. The NTE2104 employs a single transistor storage cell utilizing a dynamic control circuitry to achieve optimum performance with low power dissipation.

A unique multiplexing and latching technique for the address inputs permits the NTE2104 to be packaged in a standard 16 pin Dip.

Absolute Maximum Ratings:

Voltage on any pin relative to V_{BB} . . . . . –0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS} . . . . . –1.0V to +15V
$V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} > 0$) 0V
Operating temperature, T_A (Ambient) . . . . . 0°C to +70°C
Storage temperature (Ambient) . . . . . 0°C to +70°C
Short Circuit Output Current 50mA
Power Dissipation, P_D 1W

Recommended DC Operating Conditions: ($0°C \le T_A \le 70°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	10.8	12.0	13.2	Volts
Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts
Supply Voltage	V_{SS}	0	0	0	Volts
Supply Voltage	V_{BB}	–4.5	–5.0	–5.7	Volts
Logic 1 Voltage, RAS, CAS, WRITE	V_{IHC}	2.4	–	7.0	Volts
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.2	–	7.0	Volts
Logic 0 Voltage	V_{IL}	–1.0	–	.8	Volts

DC Electrical Characteristics:

($0°C \le T_A \le 70°C$, $V_{DD} = 12.0V \pm 10\%$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0V$; $V_{SS} = 0V$; $-5.7V \le V_{BB} \le -4.5V$)

Parameter	Symbol	Min	Typ	Max	Unit
Average V_{DD} Power Supply Current	I_{DD1}	–	–	35	mA
Standby V_{DD} Power Supply Current	I_{DD2}	–	–	2	mA
Average V_{DD} Power Supply Current During "$\overline{RAS}$ only" cycles	I_{DD3}	–	–	25	mA
		–	–	25	

DC Electrical Characteristics (Cont'd):

($0°C \leq T_A \leq 70°C$, $V_{DD} = 12.0V \pm 10\%$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0V$; $V_{SS} = 0V$; $-5.7V \leq V_{BB} \leq -4.5V$)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current	I_{CC}	–	–	–	mA
Average V_{BB} Power Supply Current	I_{BB}	–	–	150	µA
Input Leakage Current (any input)	$I_{i(L)}$	–	–	10	µA
Output Leakage Current	$I_{O(L)}$	–	–	10	µA
Output Logic 1 Voltage @ $I_{OUT} = -5mA$	V_{OH}	2.4	–	–	Volts
Output Logic 0 Voltage @ $I_{OUT} = 3.2mA$	V_{OL}	–	–	0.4	Volts
Random read or write cycle time	t_{RC}	375	–	–	ns
Read write cycle time	t_{RWC}	375	–	–	ns
Read modify write cycle time	t_{RMW}	405	–	–	ns
Page mode cycle time	t_{PC}	225	–	–	ns
Access time from row address strobe	t_{RAC}	–	–	200	ns
Access time from column address strobe	t_{CAC}	–	–	135	ns
Output buffer turn–off delay	t_{OFF}	–	–	50	ns
Row address strobe precharge time	t_{RP}	120	–	–	ns
Row address strobe pulse width	t_{RAS}	200	–	10,000	ns
Row address strobe hold time	t_{RSH}	135	–	–	ns
Column address strobe pulse width	t_{CAS}	135	–	–	ns
Column address strobe hold time	t_{CSH}	200	–	–	ns
Row to column strobe delay	t_{RCD}	25	–	65	ns
Row address set–up time	t_{ASR}	0	–	–	ns
Row address hold time	t_{RAH}	25	–	–	ns
Column address set–up time	t_{ASC}	–10	–	–	ns
Column address hold time	t_{CAH}	55	–	–	ns
Column address hold time referenced to RAS	t_{AR}	120	–	–	ns
Chip select set–up time	t_{CSC}	–10	–	–	ns
Chip select hold time	t_{CH}	55	–	–	ns
Chip select hold time reference to RAS	t_{CHR}	120	–	–	ns
Transition time (rise and fall)	t_T	3	–	50	ns
Read command set–up time	t_{RCS}	0	–	–	ns
Read command hold time	t_{RCH}	0	–	–	ns
Write command hold time	t_{WCH}	55	–	–	ns
Write command hold time referenced to RAS	t_{WCR}	120	–	–	ns
Write command pulse width	t_{WP}	55	–	–	ns

DC Electrical Characteristics (Cont'd):

($0°C \le T_A \le 70°C$, $V_{DD} = 12.0V \pm 10\%$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0V$; $V_{SS} = 0V$; $-5.7V \le V_{BB} \le -4.5V$)

Parameter	Symbol	Min	Typ	Max	Unit
Write command to row strobe lead time	t_{RWL}	70	–	–	ns
Write command to column strobe lead time	t_{CWL}	70	–	–	ns
Data in set–up time	t_{DS}	0	–	–	ns
Data in hold time	t_{DH}	55	–	–	ns
Data in hold time referenced to RAS	t_{DHR}	120	–	–	ns
Column to row strobe precharge time	t_{CRP}	0	–	–	ns
Column precharge time	t_{CP}	80	–	–	ns
Refresh period	t_{RFSH}	–	2	–	ms
Write command set–up time	t_{WCS}	0	–	–	ns
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	80	–	–	ns
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	145	–	–	ns
Data out hold time	t_{DOH}	10	–	–	μs

Pin Connection Diagram