PERICOM

Fast CMOS
18-Bit Registers

Product Features:

Common Features:

- PI74FCT16823T and PI74FCT162823T are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
  - 56-pin 240 mil wide plastic TSSOP (A)
  - 56-pin 300 mil wide palstic SSOP (V)

PI74FCT16823T Features:

- High output drive: $I_{OH} = -32$ mA; $I_{OL} = 64$ mA
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) < 1.0V
  at $V_{CC} = 5V$, $T_A = 25°C$

PI74FCT162823T Features:

- Balanced output drivers: ±24 mA
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6V
  at $V_{CC} = 5V$, $T_A = 25°C$

PI74FCT162H823T Features:

- Bus Hold retains last active bus state during 3-state
- Eliminates the need for external pull-up resistors

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16823T, PI74FCT162823T and PI74FCT162H823 are 18-bit wide registers with clock enable (x$\overline{CLKEN}$) and clear (x$\overline{CLR}$) controls that make these devices especially suitable for parity bus interfacing in high-performance systems. The devices can be operated as two 9-bit registers or one 18-bit register using the control inputs. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The PI74FCT16823T output buffers are designed with a Power-Off disable function allowing "live insertion" of boards when the devices are used as backplane drives.

The PI74FCT162823T has ±24 mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The PI74FCT162H823T has "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

Logic Block Diagram

PERICOM
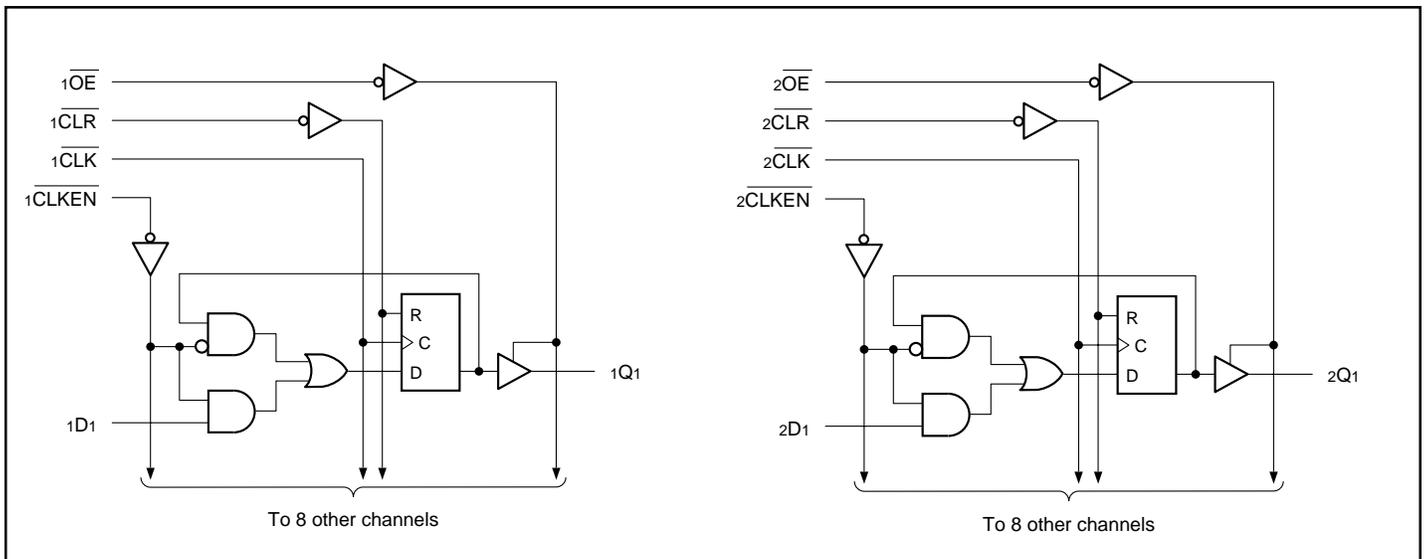
Product Pin Configuration

```
  1CLR  ▯ 1          56 ▯ 1CLK
   1OE  ▯ 2          55 ▯ 1CLKEN
   1Q1  ▯ 3          54 ▯ 1D1
   GND  ▯ 4          53 ▯ GND
   1Q2  ▯ 5          52 ▯ 1D2
   1Q3  ▯ 6          51 ▯ 1D3
   Vcc  ▯ 7          50 ▯ Vcc
   1Q4  ▯ 8          49 ▯ 1D4
   1Q5  ▯ 9          48 ▯ 1D5
   1Q6  ▯ 10         47 ▯ 1D6
   GND  ▯ 11         46 ▯ GND
   1Q7  ▯ 12  56-PIN 45 ▯ 1D7
   1Q8  ▯ 13   V56   44 ▯ 1D8
   1Q9  ▯ 14   A56   43 ▯ 1D9
   2Q1  ▯ 15         42 ▯ 2D1
   2Q2  ▯ 16         41 ▯ 2D2
   2Q3  ▯ 17         40 ▯ 2D3
   GND  ▯ 18         39 ▯ GND
   2Q4  ▯ 19         38 ▯ 2D4
   2Q5  ▯ 20         37 ▯ 2D5
   2Q6  ▯ 21         36 ▯ 2D6
   Vcc  ▯ 22         35 ▯ Vcc
   2Q7  ▯ 23         34 ▯ 2D7
   2Q8  ▯ 24         33 ▯ 2D8
   GND  ▯ 25         32 ▯ GND
   2Q9  ▯ 26         31 ▯ 2D9
   2OE  ▯ 27         30 ▯ 2CLKEN
  2CLR  ▯ 28         29 ▯ 2CLK
```
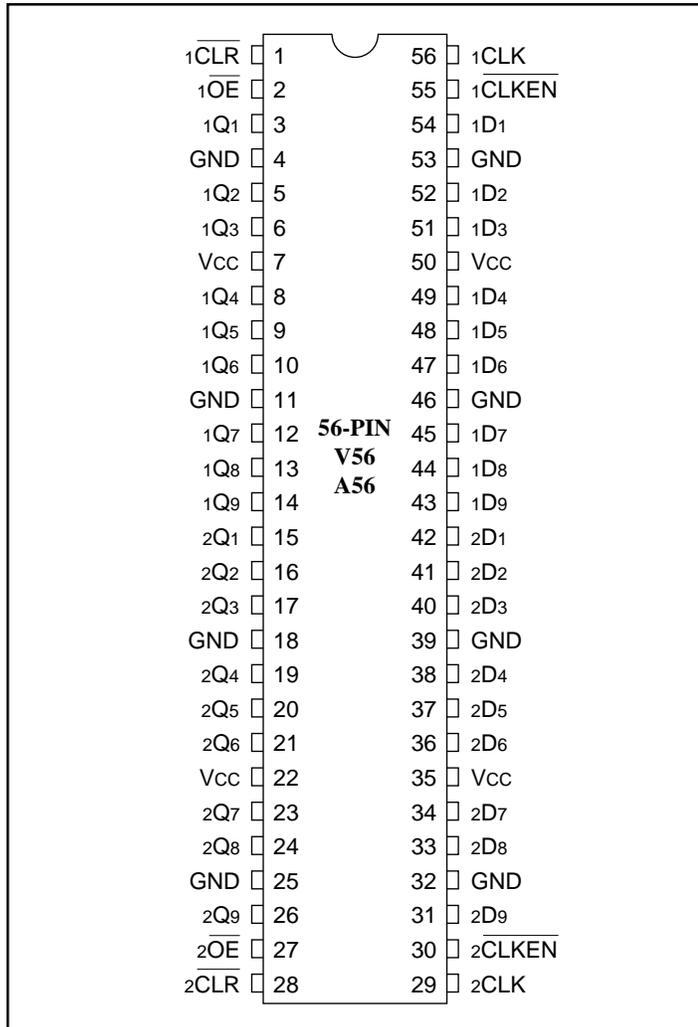
Product Pin Description

Pin Name	Description
xDx	Data Inputs[1]
xCLK	Clock Inputs
xCLKEN	Clock Enable Inputs (Active LOW)
xCLR	Asynchronous Clear Inputs (Active LOW)
xOE	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

Note: 1. For the PI74FCT162H823T, these pins have "Bus Hold." All other pins are standard, outputs, or I/Os.

PI74FCT16823 Truth Table(1)

Function	Inputs					Outputs
	xOE	xCLR	xCLKEN	xCLK	xDx	xQx
High-Z	H	X	X	X	X	Z
Clear	L	L	X	X	X	L
Hold	L	H	H	X	X	Q[2]
Load	H	H	L	↑	L	Z
	H	H	L	↑	H	Z
	L	H	L	↑	L	L
	L	H	L	↑	H	H

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH Transition
2. Output level before indicated steady-state input conditions were established.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied .... –40°C to +85°C

Supply Voltage to Ground Potential (Inputs & Vcc Only) .... –0.5V to +7.0V

Supply Voltage to Ground Potential (Outputs & D/O Only) .... –0.5V to +7.0V

DC Input Voltage .... –0.5V to +7.0V

DC Output Current 120mA

Power Dissipation 1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	Standard Input, V_{CC} = Max.	$V_{IN} = V_{CC}$			1	µA
I_{IH}	Input HIGH Current	Standard I/O, V_{CC} = Max.	$V_{IN} = V_{CC}$			1	µA
I_{IH}	Input HIGH Current	Bus Hold Input[4], V_{CC} = Max.	$V_{IN} = V_{CC}$			±100	µA
I_{IH}	Input HIGH Current	Bus Hold I/O[4], V_{CC} = Max.	$V_{IN} = V_{CC}$			±100	µA
I_{IL}	Input LOW Current	Standard Input, V_{CC} = Min.	V_{IN} = GND			–1	µA
I_{IL}	Input LOW Current	Standard I/O, V_{CC} = Min.	V_{IN} = GND			–1	µA
I_{IL}	Input LOW Current	Bus Hold Input[4], V_{CC} = Min.	V_{IN} = GND			±100	µA
I_{IL}	Input LOW Current	Bus Hold I/O[4], V_{CC} = Min.	V_{IN} = GND			±100	µA
I_{BHH}	Bus Hold	Bus Hold Input[4], V_{CC} = Min.	V_{IN} = 2.0V	–50			µA
I_{BHL}	Sustain Current		V_{IN} = 0.8V	+50			
I_{OZH}[5]	High-Impedance	V_{CC} = Max.	V_{OUT} = 2.7V			1	µA
I_{OZL}[5]	Output Current (3-State Outputs)	V_{CC} = Max.	V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max.[3], V_{OUT} = 2.5V		–50		–180	mA
V_H	Input Hysteresis				100		mV

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. This specification does not apply to bi-directional functionalities with Bus Hold.

PS2040A 03/11/96

PI74FCT16823T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = Min., V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -3.0$ mA	2.5	3.5		V
			$I_{OH} = -15.0$ mA	2.4	3.5		
			$I_{OH} = -32.0$ mA	2.0	3.0		
V_{OL}	Output LOW Voltage	$V_{CC} = Min., V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 64$ mA		0.2	0.55	V
I_{OFF}	Power Down Disable	$V_{CC} = 0V, V_{IN}$ or $V_{OUT} \leq 4.5V$		—	—	±100	µA

PI74FCT162823T/162H823T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = Min., V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -24.0$ mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	$V_{CC} = Min., V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 24$ mA		0.3	0.55	V
I_{ODL}	Output LOW Current	$V_{CC} = 5V, V_{IN} = V_{IH}$ OR $V_{IL}, V_{OUT} = 1.5V$[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5V, V_{IN} = V_{IH}$ OR $V_{IL}, V_{OUT} = 1.5V$[3]		−60	−115	−150	mA

Capacitance ($T_A = 25°C$, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	5.5	8	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	1.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $x\overline{OE}$ = $x\overline{CLKEN}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz	V_{IN} = V_{CC} V_{IN} = GND		0.8	2.7	mA
		50% Duty Cycle $x\overline{OE}$ = $x\overline{CLKEN}$ = GND f_I = 5 MHz One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND		1.3	3.2	
		V_{CC} = Max., Outputs Open f_{CP} = 10 MHz	V_{IN} = V_{CC} V_{IN} = GND		4.2	7.1[5]	
		50% Duty Cycle $x\overline{OE}$ = $x\overline{CLKEN}$ = GND Eighteen Bits Toggling f_I = 2.5 MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND		9.2	22.1[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V).
   D_H = Duty Cycle for TTL Inputs High.
   N_T = Number of TTL Inputs at D_H.
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f .
   All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16823T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	16823AT Com. Min	Max	16823BT Com. Min	Max	16823CT Com. Min	Max	16823DT Com. Min	Max	16823ET Com. Min	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay xCLK to xQx	$C_L = 50$ pF $R_L = 500\Omega$	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	4.4	ns
		$C_L = 300$ pF[3] $R_L = 500\Omega$	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	1.5	8.0	ns
t_{PHL}	Propagation Delay $\overline{xCLR}$ to xQx	$C_L = 50$ pF $R_L = 500\Omega$	1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	1.5	4.4	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{xOE}$ to xQx	$C_L = 50$ pF $R_L = 500\Omega$	1.5	12.0	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns
		$C_L = 300$ pF[3] $R_L = 500\Omega$	1.5	23.0	1.5	15.0	1.5	12.5	1.5	10.0	1.5	9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{xOE}$ to xQx	$C_L = 5$ pF[3] $R_L = 500\Omega$	1.5	7.0	1.5	6.5	1.5	6.2	1.5	5.0	1.5	4.0	ns
		$C_L = 50$ pF $R_L = 500\Omega$	1.5	8.0	1.5	7.5	1.5	6.5	1.5	5.0	1.5	4.0	ns
t_{SU}	Setup Time HIGH or LOW, xDx to xCLK	$C_L = 50$ pF $R_L = 500\Omega$	4.0	—	3.0	—	3.0	—	3.0	—	1.5	—	ns
t_H	Hold Time HIGH or LOW, xDx to xCLK		2.0	—	1.5	—	1.5	—	1.5	—	0	—	ns
t_{SU}	Setup Time HIGH or LOW, $\overline{xCLKEN}$ to xCLK		4.0	—	3.0	—	3.0	—	3.0	—	2.5	—	ns
t_H	Hold Time HIGH or LOW, $\overline{xCLKEN}$ to xCLK		2.0	—	0	—	0	—	0	—	0	—	ns
t_W	xCLK Pulse Width HIGH or LOW[3]		7.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
t_W	$\overline{xCLR}$ Pulse Width LOW[3]		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
t_{REM}	Recovery Time[3] $\overline{xCLR}$ to xCLK		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
$t_{SK(O)}$	Output Skew [4]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PS2040A 03/11/96

PI74FCT162823T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	162823AT Com.		162823BT Com.		162823CT Com.		162823DT Com.		162823ET Com.		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay xCLK to xQx	$C_L = 50$ pF $R_L = 500\Omega$	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	4.4	ns
		$C_L = 300$ pF[3] $R_L = 500\Omega$	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	1.5	8.0	ns
t_{PHL}	Propagation Delay x$\overline{CLR}$ to xQx	$C_L = 50$ pF $R_L = 500\Omega$	1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	1.5	4.4	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xQx	$C_L = 50$ pF $R_L = 500\Omega$	1.5	12.0	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns
		$C_L = 300$ pF[3] $R_L = 500\Omega$	1.5	23.0	1.5	15.0	1.5	12.5	1.5	10.0	1.5	9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] x$\overline{OE}$ to xQx	$C_L = 5$ pF[3] $R_L = 500\Omega$	1.5	7.0	1.5	6.5	1.5	6.2	1.5	5.0	1.5	4.0	ns
		$C_L = 50$ pF $R_L = 500\Omega$	1.5	8.0	1.5	7.5	1.5	6.5	1.5	5.0	1.5	4.0	ns
t_{SU}	Setup Time HIGH or LOW, xDx to xCLK	$C_L = 50$ pF $R_L = 500\Omega$	4.0	—	3.0	—	3.0	—	3.0	—	1.5	—	ns
t_H	Hold Time HIGH or LOW, xDx to xCLK		2.0	—	1.5	—	1.5	—	1.5	—	0	—	ns
t_{SU}	Setup Time HIGH or LOW, x$\overline{CLKEN}$ to xCLK		4.0	—	3.0	—	3.0	—	3.0	—	2.5	—	ns
t_H	Hold Time HIGH or LOW, x$\overline{CLKEN}$ to xCLK		2.0	—	0	—	0	—	0	—	0	—	ns
t_W	xCLK Pulse Width HIGH or LOW[3]		7.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
t_W	x$\overline{CLR}$ Pulse Width LOW[3]		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
t_{REM}	Recovery Time[3] x$\overline{CLR}$ to xCLK		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
$t_{SK(O)}$	Output Skew [4]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT162H823T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	162H823AT Com. Min	Max	162H823BT Com. Min	Max	1628H23CT Com. Min	Max	162H823DT Com. Min	Max	162H823ET Com. Min	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay xCLK to xQx	$C_L = 50\,pF$ $R_L = 500\,\Omega$	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	4.4	ns
		$C_L = 300\,pF^{(3)}$ $R_L = 500\,\Omega$	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	1.5	8.0	ns
t_{PHL}	Propagation Delay xCLR to xQx	$C_L = 50\,pF$ $R_L = 500\,\Omega$	1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	1.5	4.4	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{xOE}$ to xQx	$C_L = 50\,pF$ $R_L = 500\,\Omega$	1.5	12.0	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns
		$C_L = 300\,pF^{(3)}$ $R_L = 500\,\Omega$	1.5	23.0	1.5	15.0	1.5	12.5	1.5	10.0	1.5	9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{xOE}$ to xQx	$C_L = 5\,pF^{(3)}$ $R_L = 500\,\Omega$	1.5	7.0	1.5	6.5	1.5	6.2	1.5	5.0	1.5	4.0	ns
		$C_L = 50\,pF$ $R_L = 500\,\Omega$	1.5	8.0	1.5	7.5	1.5	6.5	1.5	5.0	1.5	4.0	ns
t_{SU}	Setup Time HIGH or LOW, xDx to xCLK	$C_L = 50\,pF$ $R_L = 500\,\Omega$	4.0	—	3.0	—	3.0	—	3.0	—	1.5	—	ns
t_H	Hold Time HIGH or LOW, xDx to xCLK		2.0	—	1.5	—	1.5	—	1.5	—	0	—	ns
t_{SU}	Setup Time HIGH or LOW, xCLKEN to xCLK		4.0	—	3.0	—	3.0	—	3.0	—	2.5	—	ns
t_H	Hold Time HIGH or LOW, xCLKEN to xCLK		2.0	—	0	—	0	—	0	—	0	—	ns
t_W	xCLK Pulse Width HIGH or LOW[3]		7.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
t_W	xCLR Pulse Width LOW[3]		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
t_{REM}	Recovery Time[3] $\overline{xCLR}$ to xCLK		6.0	—	6.0	—	6.0	—	6.0	—	3.0	—	ns
$t_{SK(O)}$	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PS2040A 03/11/96