Austria Mikro Systeme International AG

DIGITAL TIME/SPACE CROSSPOINT SWITCH

Key Features

- 8-Line x 32 PCM Channel Inputs
- 8-Line x 32 PCM Channel Output
- 256 Ports Non Blocking Time/Space Crosspoint Switch
- Single Power Supply of 5V
- Low Power Consumption
- Microprocessor Control Interface
- Open Drain Serial Outputs
- CMOS Process
- Simultaneous Connection/Disconnection under Microprocessor Control
- Extraction/Insertion of Single PCM Channels
- Channel Zero Extraction

General Description

AS3588A is designed for switching PCM channels under microprocessor control in digital exchanges, PBX or Central Office equipment. It provides a non blocking digital switching matrix for up to 256x256 64 kbit/sec channels.

Each of the eight serial inputs and outputs consists of 32 64 kbit/sec channels multiplexed to/from a 2048 kbit/sec serial PCM bit stream.

Simultaneously it allows its controlling microprocessor to read PCM output channels or to write to PCM output channels.

Ordering Information

Part Number	Package
AS3588AP	40 Pin DIP
AS3588AQ	44 QFP

Block Diagramme

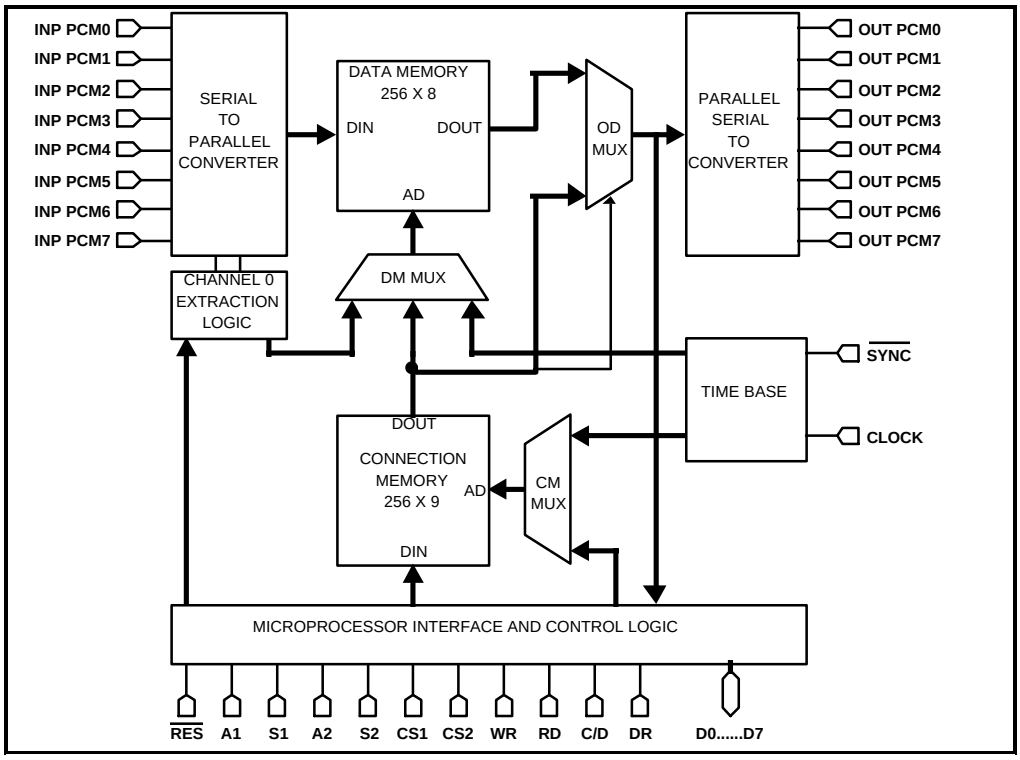
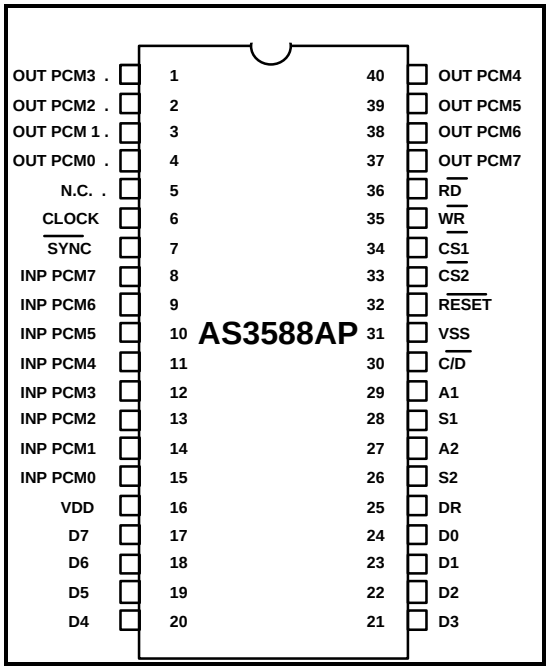


Figure 1: Block Diagramme

Pinout Configuration



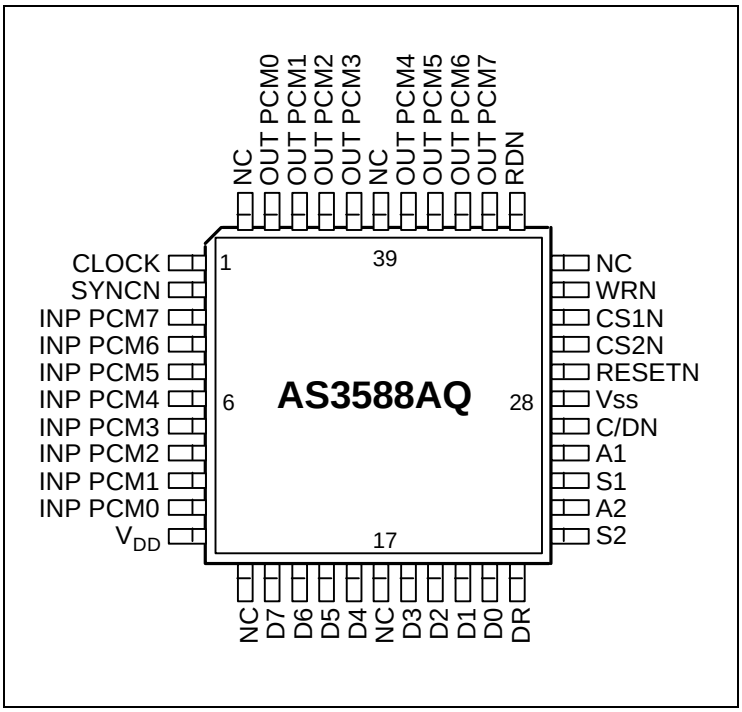


Figure 2: Pinout 40 pin DIP and 44 pin QFP

Pin Description

DIP	QFP	Type	Symbol	Description
1 - 4	40 - 43	OP	OUTPCM3 to OUTPCM0	**PCM Outputs 3 to 0**. These are open drain outputs for four primary rate PCM output streams.
5	44, 12, 17, 33, 39	-	N.C.	Unused Pin
6	1	IP	CLOCK	**Master Clock Input** This signal is the timing reference for all internal operations. The PCM bit cell boundaries lie on the alternate rising edges of this clock.
7	2	IP	SYNC	**Synchronization Input** This is an edge sensitive input for frame synchronization in the PCM bit stream with a typical repetition rate of 8 kHz. The rising edge determines the start of a new frame.
8 - 15	3 - 10	IP	INPPCM7 to INPPCM0	**PCM Inputs 7 to 0** These are the inputs for primary rate PCM input streams
16	11	Power	VDD	**Positive Supply Voltage**
17 - 24	13 - 16, 18 - 21	I/O	D7 to DO	**Data Bus I/O Port**. These are the bi-directional data pins to the microprocessor interface. Only 5 bits are used when data is written into AS3588A (D4 to D0)
25	22	OP	DR	**Data Ready Output.** This active high signal goes low for signalling purposes

26 - 27	23 - 26	IP	A1, S1, A2, S2	**Address Decoder Inputs** These active high inputs are provided for larger non blocking digital switching matrixes with cascaded AS 3588 devices.
30	27	IP	C/D	**Control/ Data Select Input** The signal on this control input defines whether the data on the data bus should be interpreted as opcode or as data. During a write operation a low signal defines the bus content as data and a high signal defines it as opcode. During a read operation this input acts as multiplexing control: OR1 is selected by a low signal; OR2 is selected by a high signal.
31	28	Power	VSS	**Negative Supply Voltage**
32	29	IP	RESET	**Reset Input** This active low input is used for starting the system initialization. This pin is strobed at the first timeslot. The initialization routine takes one time frame period independent of the reset pulse width and is continued for another time frame when the signal is kept low during strobe. Initialization disables the output drivers of the microprocessor interface; The Connection Memory is cleared and the PCM output drivers are disabled.
33 - 34	30 - 31	IP	CS1, CS2	**Chip Select Inputs** These are the inputs for the active low chip selects on the microprocessor interface. The two inputs are provided for flexible decoding.
35	32	IP	WR	**Write Input** This active low input is for the write signal on the microprocessor interface. The data bus is strobed on the rising edge.
36	34	IP	RD	**Read Input** This active low input is for the read signal on the microprocessor interface. The databus is updated on the falling edge.
37 - 40	35 - 38	OP	OUTPCM 7 to OUTPCM 4	**PCM Outputs 7 to 4** These are open drain outputs for four primary rate PCM output streams.

Functional Description

The AS3588A is a digital time / space crosspoint switching matrix and is designed to switch data from eight primary rate input ports operating at 2048 kbit/s to eight primary rate 2048 kbit/s output ports. Simultaneously it allows its controlling microprocessor to read PCM output channels or write to PCM output channels (Messaging). To the Microprocessor AS3588A looks like a memory mapped peripheral device that is controlled by six different instructions. It can write to AS3588A commands to establish or release switched connections between PCM input channels and PCM output channels or to transmit messages on specific PCM output channels. By reading from the AS3588 the microprocessor can receive messages from PCM output channels or from the channel 0 of the input ports or check which connections have been made by reading the connection memory.

By integrating both switching and interprocessor communications the AS3588A is ideally suited for distributed processing in digital switching systems.

Hardware Description

Timing

All AS3588 internal timing is derived from the 4.096 MHz master clock signal CK and the 8 kHz frame synchronization signal SYNC. Different time bases for the serial to parallel PCM input converter and the parallel to serial PCM output converter are generated internally which compensate for the internal input/output conversion delays. They are synchronized to a preset number in order to restore the channel and bit se-

quential addressing information. The count difference between the bases is 32 which is two time slots, the minimum PCM propagation time. The device activates the output channels one bit time before input channels are strobed. This feature allows inputs and outputs to be tied together cancelling any analogue delay of digital outputs up to a time which is specified in the timing diagramme.

Serial Input PCM Conversion

Serial data at 2048 kbit/sec is received at the eight PCM inputs INP PCM1 to INP PCM7. Each serial port accepts 32 64 kbit channels of data, each channel containing an 8-bit word which may represent a PCM-encoded analogue/voice sample as provided by a codec (e.g. AMS` S44231 to S44238 or AS3554 to AS3569 codec family). This serial input word is converted into parallel data by a serial to parallel PCM converter.

Data Memory and Connection Memory

The parallel data is stored in the 256 x 8 Data Memory which is updated every frame period. The locations in the Data Memory are associated with particular channels in particular PCM input ports. The locations in the 256 x 9 Connection Memory are associated with particular PCM output streams. These locations can be accessed by the microprocessor which controls the device. When a channel is due to be transmitted on a PCM output stream the data can either be switched from a PCM input channel in space (INP PCM1 to INP PCM7)) or time (slot 1 to 32). In this case the 9^{th} bit in the control memory is set to "0". Alternatively it can originate from the Connection Memory. In this case the 9^{th} bit of the control memory is set to "1". If the data is switched from an input, the contents of the Connection Memory associated with the output channel is used to point to the Data Memory locations. This Data Memory address corresponds to the channel of the PCM input stream on which the data for switching has arrived. If the data for the output channel originates from the microprocessor then the contents of the Connection Memory associated with the PCM output Channel are output directly and this data is output as message constantly once every frame until the microprocessor intervenes.

Serial Output PCM Conversion

The parallel channel data is converted back into a serial PCM stream by a parallel to serial PCM converter and is transmitted at the eight PCM output ports OUT PCM1 to OUT PCM7.

Microprocessor Interface

The asynchronous microprocessor interface is controlled by 9 control signals (WR, RD, CS1, CS2, A1, S1, A2, S2, DR) and provides data and instruction transfer via the 8-bit data bus (D7 to D0). For each of the six available operations two to four data bytes and one instruction byte are written into a five level deep stack. After a check of the correctness the function is executed. Data bytes are defined by a low level on the C/D input while a command byte is defined by a high level. The active high Data Ready output pin of AS3588 provides a handshake signal to the microprocessor when transfer information is ready. During long instructions like an initialization routine after RESET or execution of instruction 6 only valid opcodes with the associated datafield are accepted; the execution of the new instruction is started after the current instruction has been completed. Memory content and status information can be extracted by reading the two internal registers OR1 and OR2 and using C/D as multiplexing control signal. OR1 is selected by a low level on the C/D input and contains either data from the data memory or the connection memory. OR2 is selected with a high level and contains the opcode and additional status information. Read operations are only executed if the device is fully selected with CS1=CS2=0 and A1=S1 and A2=S2. There are no restrictions on the sequence of read and write operations as long as only one of the control pins (RD, WR) is selected. If both pins are pulled low, the interface bus goes into high impedance state. The register contents is maintained as long as this condition persists and is updated 3 cycles after a new opode or an OR2 read. Single or multiple read operations of OR1 and OR2 should be carried out with separate read strobes which are responsible of stepping through the instruction flow.

Software Control

AS3588A performs two switching functions and four auxiliary functions for diagnostic purposes and data insertion from the microprocessor interface.

1) PCM CHANNEL CONNECTION

This function connects a PCM input channel to a PCM output channel. The control information from the microprocessor consists of four data bytes and one command byte. Byte one and two contain information about the PCM input line and PCM input channel that is written into the connection memory. Byte three and four contain information on the PCM output line and the PCM output channel and act as address to the specific connection memory location. If AS3588 is selected by CS1=CS2=0 and if the condition A1=S1 and A2=S2 is met, the command instruction is executed as defined. If the device is selected by CS1 and CS2 only this command will perform a disconnect function on the specific output channel. If the instruction code was found to be invalid, DR is driven low until a valid instruction code is supplied; the registers are not modified.

2) PCM CHANNEL DISCONNECTION

This function disconnects a PCM output channel. The control information from the microprocessor consists

of two data bytes and one command byte. Byte one and two contain information about the PCM output line and the PCM output channel and act as address pointer to the specific connection memory location. The command instruction is only executed if AS3588A is selected by CS1=CS2=0 and if the condition A1=S1 and A2=S2 is met. If the device is only selected by CS1 and CS2. this command is not executed and DR remains high. If the instruction code was found to be invalid, DR is driven low until a valid instruction code is supplied; the registers are not modified.

3) BYTE INSERTION INTO A PCM OUTPUT CHANNEL / CHANNEL DISCONNECTION

This function inserts a single byte from the microprocessor into a PCM output channel. The control information from the microprocessor consists of four data bytes and one command byte. Byte one and two contain the message byte from the microprocessor which is stored in a connection memory location. Byte three and four contain information about the PCM output line and the PCM output channel and act as address to the specific connection memory location where the message byte that is contained in byte1 and byte 2 is stored. If AS3588A is selected by CS1, CS2 and if the condition A1=S1 and A2=S2 is met, the command instruction is executed as defined. If the device is selected by CS1 and CS2 only this command will perform a disconnect function on the specific output channel. If the instruction code was found to be invalid, DR is driven low until a valid instruction code is supplied; the registers are not modified.

4) PCM OUTPUT CHANNEL EXTRACTION

This function extracts a specific output channel and transfers it to the microprocessor bus. PCM input channels can be extracted by connecting the channels to output channels with instruction 1. The control information from the microprocessor consists of two data bytes and one command byte. Byte one and two contain information about the PCM output line and the PCM output channel. The extracted channel is stored in the OR1 register. The command instruction is only executed if AS3588A is selected by CS1=CS2=0 and if the condition A1=S1 and A2=S2 is met. If the device is only selected by CS1 and CS2. this command is not executed and DR remains high.

If the instruction code was found to be invalid, DR is driven low until a valid instruction code is supplied; the registers are not modified.

5) TRANSFER OF A CONNECTION MEMORY LOCATION

This function allows the access of the contents of a connection memory location associated to a specific PCM output channel and transfers it to the microprocesor bus. The control information from the microprocesor consists of two data bytes and one command byte. Byte one and two contain information about the PCM output line and the PCM output channel. The connection memory bits C7 to C0 are stored in register OR1, C8 is stored in register OR2. If C8=0 the remaining eight bits contain information about the connected PCM input channel. If C8=1, the remaining bits can be all log. "1" if the output channel is not connected to an input channel and if it was not modified by the microprocessor. If C8=1 but the remaining bits are not all set to log. "1" they contain a message byte from an active output channel which was loaded by the byte insertion instruction 3. DR goes low for two clock cycles in that case. The command instruction is executed if AS3588A is selected by CS1=CS2=0. If the instruction code was found to be invalid, DR is driven low until a valid instruction code is supplied; the registers are not modified.

6) TRANSFER OF 0 CHANNEL PCM DATA FROM SELECTED PCM INPUTS

This function is used to extract the contents of channel 0 of the PCM inputs which do not contain "01" in the two most significant bits. The control information from the microprocessor consists of two data bytes and one command byte. Byte one and two contain information about the PCM input selection mask byte. The contents of channel 0 are available from the OR1 register from which the microprocessor can transfer them by successive reads from the same register. To enable instruction 6 it is necessary to read register OR2. This is because instruction 6, used between other short instructions of type 1 to 5 , must have a lower priority and can be enabled only after the short instructions have been completed. Instruction 6 normally has a long process and a special flow: First a not-all-zero mask field is stored in the "expected messages" register and in another "background" register. A logic "1" means an input bus enabling condition, a log. "0" means an input bus disabling condition. This operation starts the second phase of instruction 6 which is called "channel 0 extraction" and is repeated at the beginning of any new time frame. At the beginning of the time frame a new copy of activated channels to be extracted is made from the "background register"' and put in the "expected messages" register. In addition the latter register is modified to indicate the exact number of messages that have arrived. The term messages covers any input 0 channel data with starting sequence different from "01". Using this signature the number of expected messages can be reduced to correspond to the number of effective messages. If and only if the residual number is different from zero will the device start the extraction protocol at the end of the current routine. The procedure is as follows:

The DR output is pulsed low for two clock cycles as interrupt request to the microprocessor and OR2 is loaded with the total number of active channels to be extracted. The transfer of OR2 content to the microprocessor continues the extraction which consists of repeated steps of OR1 and OR2 loading indicating respectively the message and the incoming bus number.

Reading the registers in the order OR1 , OR2 must be continued until completion or until the time frame runs out. With a new time frame a new extraction process begins, resuming the copy operation from the background register. During extraction the active channels are scanned from the highest to the lowest number (from 7 to 0). While extraction is being carried out the time interval requirements between active rising edges of RD are minimum 5 to 13 tCK for sequence OR2- OR1 and minimum 3 times tCK for sequence OR1 - OR2. Channel 0 extraction is disabled by a reset pulse or by writing a zero mask into the device. This clears the mask register and the background register

Instruction Tables

Instruction 1: Channel Connection / Disonnection

Control Signals					Data Bus								Comments
SEL	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	BI2	BI1	BI0	Byte 1: PCM input line
X	0	0	0	1	X	X	X	CI4	CI3	CI2	CI1	CI0	Byte2: PCM input channel
X	0	0	0	1	X	X	X	X	X	BO2	BO1	BO0	Byte 3: PCM output line
X	0	0	0	1	X	X	X	CO4	CO3	CO2	CO1	CO0	Byte4: PCM output channel
1/0	1	0	0	1	X	X	X	X	0	0	0	1	Instruction Byte
1	0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	OR1
					(BI2)	(BI1)	(BI0)	(CI4)	(CI3)	(CI2)	(CI1)	(CI0)	Contents of CM
					(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	Note 1
1	1	0	1	0	A7	A6	A5	C8	OP3	OP2	OP1	OP0	OR2
					(BO2)	(BO1)	(BO0)	(0)	(0)	(0)	(0)	(1)	
					(BO2)	(BO1)	(BO0)	(1)	(0)	(0)	(0)	(1)	Note 1

Note1: The Connection memory contains all ones if not connected

Instruction 2: Output Channel Disconnection

Control Signals					Data Bus								Comments
SEL	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	BO2	BO1	BO0	Byte 1: PCM output line
X	0	0	0	1	X	X	X	CO4	CO3	CO2	CO1	CO0	Byte 2: PCM output channel
1	1	0	0	1	X	X	X	X	0	0	1	0	Instruction Byte
1	0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	OR1
					(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	Note 1
1	1	0	1	0	A7	A6	A5	C8	OP3	OP2	OP1	OP0	OR2
					(BO2)	(BO1)	(BO0)	(1)	(0)	(0)	(1)	(0)	

Note1: The Connection memory contains all ones if not connected

Instruction 3: Channel Insertion

Control Signals					Data Bus								Comments
SEL	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	CI7	CI6	CI5	Byte 1: 3 MSB of byte
X	0	0	0	1	X	X	X	CI4	CI3	CI2	CI1	CI0	Byte 2: 5 LSB´s of byte
X	0	0	0	1	X	X	X	X	X	BO2	BO1	BO0	Byte 3: PCM output line
X	0	0	0	1	X	X	X	CO4	CO3	CO2	CO1	CO0	Byte 4: PCM output channel
1/0	1	0	0	1	X	X	X	X	0	1	0	0	Instruction Byte
1	0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	OR1
					(CI7)	(CI6)	(CI5)	(CI4)	(CI3)	(CI2)	(CI1)	(CI0)	Contents of CM
					(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	Note 1
1	1	0	1	0	A7	A6	A5	C8	OP3	OP2	OP1	OP0	OR2
					(BO2)	(BO1)	(BO0)	(1)	(0)	(1)	(0)	(0)	

Note1: The Connection memory contains all ones if not connected

Instruction 4: Output Channel Extraction

Control Signals					Data Bus								Comments
SEL	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	BO2	BO1	BO0	Byte 1: PCM output bus
X	0	0	0	1	X	X	X	CO4	CO3	CO2	CO1	CO0	Byte 2: PCM output channel
1	1	0	0	1	X	X	X	X	1	0	1	1	Instruction Byte
1	0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	OR1: Memory Contents
1	1	0	1	0	A7	A6	A5	C8	OP3	OP2	OP1	OP0	OR2
					(BO2)	(BO1)	(BO0)	(1)	(1)	(0)	(1)	(1)	Data is from CM
					(BO2)	(BO1)	(BO0)	(0)	(1)	(0)	(1)	(1)	Data is from DM

Instruction 5: Connection Memory Extraction

Control Signals					Data Bus								Comments
SEL	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	BO2	BO1	BO0	Byte 1: PCM output line
X	0	0	0	1	X	X	X	CO4	CO3	CO2	CO1	CO0	Byte 2: PCM output channel
X	1	0	0	1	X	X	X	X	1	0	0	0	Instruction Byte
1	0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	OR1: LSB of CM
1	1	0	1	0	A7	A6	A5	C8	OP3	OP2	OP1	OP0	OR2: MSB of CM
					(BO2)	(BO1)	(BO0)	C8	(1)	(0)	(0)	(0)	Data is from CM

Instruction 6: Channel 0 Extraction

Control Signals					Data Bus								Comments
SEL	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	MI7	MI6	MI5	Byte 1: MSB of selection mask
X	0	0	0	1	X	X	X	MI4	MI3	MI2	MI1	MI0	Byte 2: LSB of selection mask
1	1	0	0	1	X	X	X	X	1	1	1	0	Instruction Byte
Mask Store Control													
1	0	0	1	0	X	X	X	X	X	X	X	X	OR1: unchanged
1	1	0	1	0	N2	N1	N0	TN	1	1	1	0	OR2: see Note 1
First Data Transfer													
1	0	0	1	0	X	X	X	X	X	X	X	X	OR1: unchanged
1	1	0	1	0	N2	N1	N0	Tn	1	1	1	0	OR2: see Note 2
Repeated Data Transfer													
1	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0	OR1: expected message
1	1	0	1	0	P2	P1	P0	Fn	1	1	1	0	OR2: See Note 3

Note 1: Reading OR 2 is optional after mask store or redefinition, because the instruction is only activated by a not zero mask
Note 2: After the mask store operation (N2 N1 N0) is the sum of activated channels; after DR it is the sum of active channels; Tn = 1 means activation of the function after mask store. After DR only Tn=1 can appear to flag a not zero mask writing.
Note 3: Reading of OR2 is mandatory after DR in order to step the data transfer; reading OR1 is also needed to scan in the descending order of priority. Only relevant messages are considered, that means only messages with a signature different from 01. (P2 P1 P0) is the PCM bus on which the message in OR1 was found; Fn is a continuation bit which flags with a 1/0 level more / no more extraction will be performed.

Electrical Characteristics

Absolute Maximum Ratings*

Supply Voltage ..... -0.3²VCC²7V

Voltage on Digital Inputs ..... -0.3V²VIN²VCC+0.3V

Voltage on Digital Outputs ..... Vout²VCC+0.3V

Total Package Power Dissipation 1.5W

Storage Temperature Range ..... -65 to +150 °C

*Exceeding these figures may cause permanent damage. Functional operation under these conditions is not permitted

Recommended Operating Conditions: Voltages are with respect to ground (VSS) unless otherwise noted

Symbol	Parameter	Condition	Min.	Typ.*	Max.	Units
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
T_{OP}	Operating Temperature		0		+85	°C
V_{IN}	Input Voltage		0		VDD	V
fC	Input Clock Frequency			4.096		MHz
fSYNC	Frame Sync. Frequency			8		kHz

Typical Figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing

DC Characteristics: Clocked operation over recommended temperature and voltage range

Symbol	Parameter	Condition	Min.	Typ.*	Max.	Units
VIL	Input Low Level		-0.3		0.8	V
VIH	Input High Level		2.0		VCC	V
VOL	Output Low Level	IOL=1.8 mA			0.4	V
VOH	Output High Level	IOH=250 µA	2.4			V
VOL	PCM Output Low Level	IOL=3.0 mA			0.4	V
IIL	Input Leakage Current	0V²VIN²VCC			10	µA
IDL	Data Bus Leakage Current VCC applied; Pin35,36 to VCC after Initializing	0V²VIN²VCC; -10		+10	µA	
ICC	Operating Current	FC= 4.096 MHz		5	12	mA

Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing
All DC characteristics are valid 250µs after VCC and clock have been applied

AC Electrical Characteristics

Capacitances: Operation over recommended temperature and voltage range

Symbol	Parameter	Condition	Min.	Typ.*	Max.	Units
CI	Input Capacitance	f= 1MHz			5	pF
CI/O	I/O Capacitance	f= 1MHz			15	pF
CO	Output Capacitance	f= 1MHz			10	pF

Note: unused pins are connected to VSS

Clock Timing Characteristics (Figure 3): Operation over recommended temperature and voltage range

Symbol	Parameter	Condition	Min.	Typ.*	Max.	Units
tCK	Clock Period		230	244		ns
tWLCK	Clock Low Level Width		100			ns
tWHCK	Clock High Level Width		100			ns
tRCK	Clock Rise Time				25	ns
tFCK	Clock Fall Time				25	ns
tSY	Sync. Period			125		µs
tSLSY	Sync. Low Setup Time		80			ns
tHLSY	Sync. Low Hold Time		40			ns
tSHSY	Sync. High Setup Time		80			ns
tWHSY	Sync. High Level Width		tCK			ns

Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing

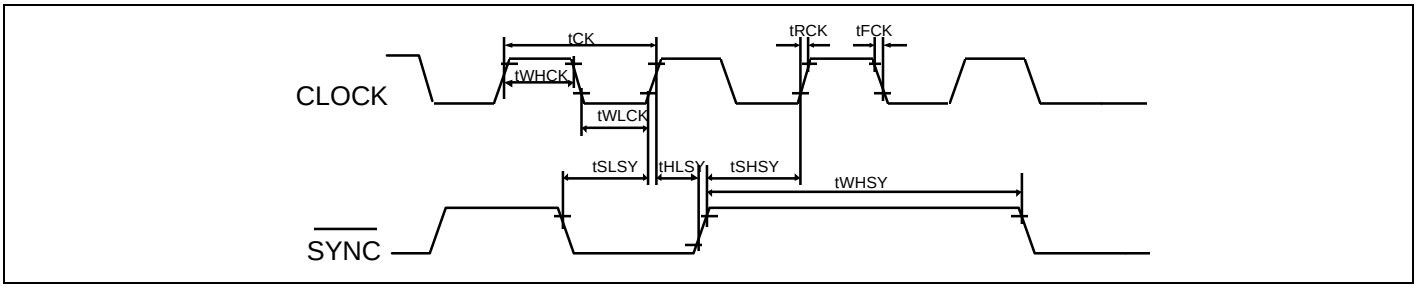


Figure 2

Figure 3. Clock Timing

PCM Timing Characteristics (Figure 4): Operation over recommended temperature and voltage range

Symbol	Parameter	Condition	Min.	Typ.*	Max.	Units
tSPCM	PCM IN Setup Time		10			ns
tHPCM	PCM IN Hold Time		45			ns
tPDLPCM	PCM OUT Delay Time	CL=50pF, RL=2k½	45			ns
tPDHPCM	PCM OUT Delay Time	CL=50pF, RL=2k½			200	ns

Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing

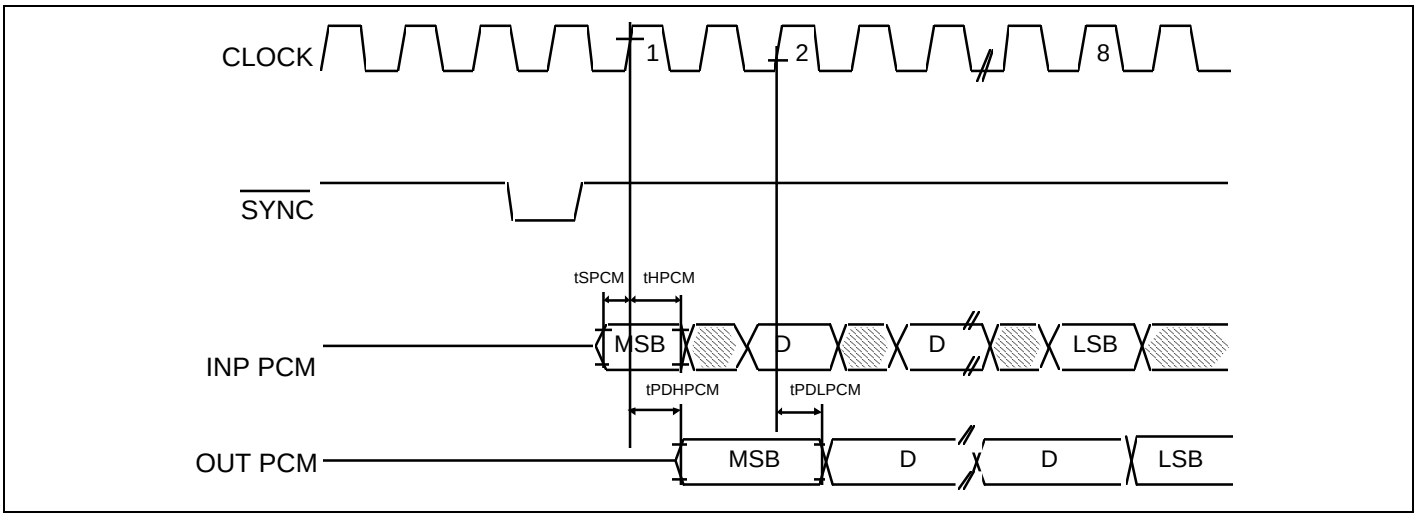


Figure 4. PCM Timing

Reset Timing Characteristics (Figure 5): Operation over recommended temperature and voltage range

Symbol	Parameter	Condition	Min.	Typ.*	Max.	Units
tSLRES	Reset Low Setup Time		100			ns
tHLRES	Reset Low Hold Time		50			ns
tSHRES	Reset High Setup Time		90			ns
tWHRES	Reset High Level Width		tCK			ns

Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing

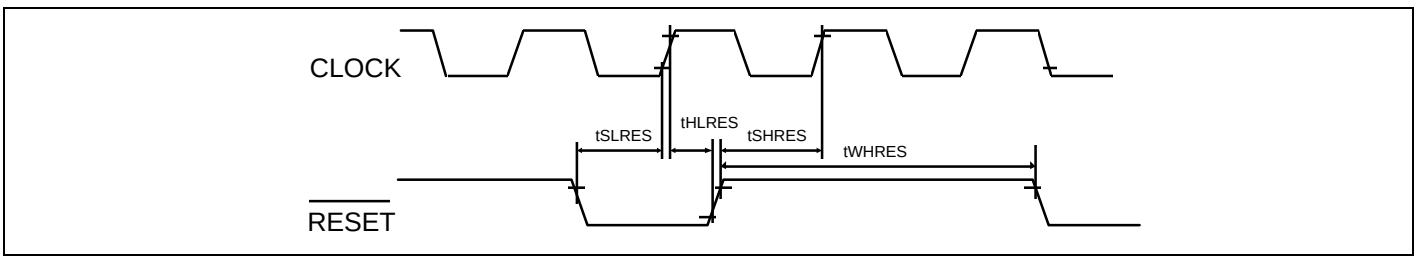


Figure 5 Reset Timing

Write Timing Characteristics (Figure 6): Operation over recommended temperature and voltage range

Symbol	Parameter	Condition	Min.	Typ.*	Max.	Units
tWLWR	Write Pulse Low Width		150			ns
tWHWR	Write Pulse High Width		tCK			ns
tREP	Repetition Interval between active Write Pulses	tREP=40+2 tCK+tWLCK + tRCK		see formula		ns
tSHRD	High Level Setup Time to active Read Pulse		0			ns
tHHRD	High Level Hold Time from active Read Pulse		20			ns
tRWR	Write Pulse Rise Time				60	ns
tFWR	Write Pulse Fall Time				60	ns
tSLCSWR	CS Low Setup Time to WR Falling Edge	Active State	0			ns
tHLCSWR	CS Low Hold time from WR Rising Edge	Active State	0			ns
tSHCSWR	CS High Setup Time to WR Falling Edge	Inative State	0			ns
tHHCSWR	CS High Hold Time from WR Rising Edge	Inactive State	0			ns
tSCDWR	C/D Setup Time to Write Pulse End		130			ns
tHCDWR	C/D Hold Time from Write Pulse End		25			ns
tSASWR	Address Select Setup Time to Write Pulse End		130			ns
tHASWR	Adress Select Hold Time from Write Pulse End		25			ns
tWDR	Data Ready Low Time	Opcodes 5, 6			2 tCK	ns
tPDDR	Data Ready Delay Time from Write Pulse End	Opcode 5; CL=50pF Active Opcode	5 tCK		14 tCK	
tSDWR	Data Setup Time to Write PulseEnd		130			ns
tHDWR	Data Hold Time from Write Pulse End		25			ns

Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing

Note: Because of internal clock re-synchronization one single additional requirement is recommended in order to produce a simultaneous instruction execution in a multi-chip configuration: WR rising edge has to be 20 to 20 + tWL(cK) nsec late relative to clock falling edge.

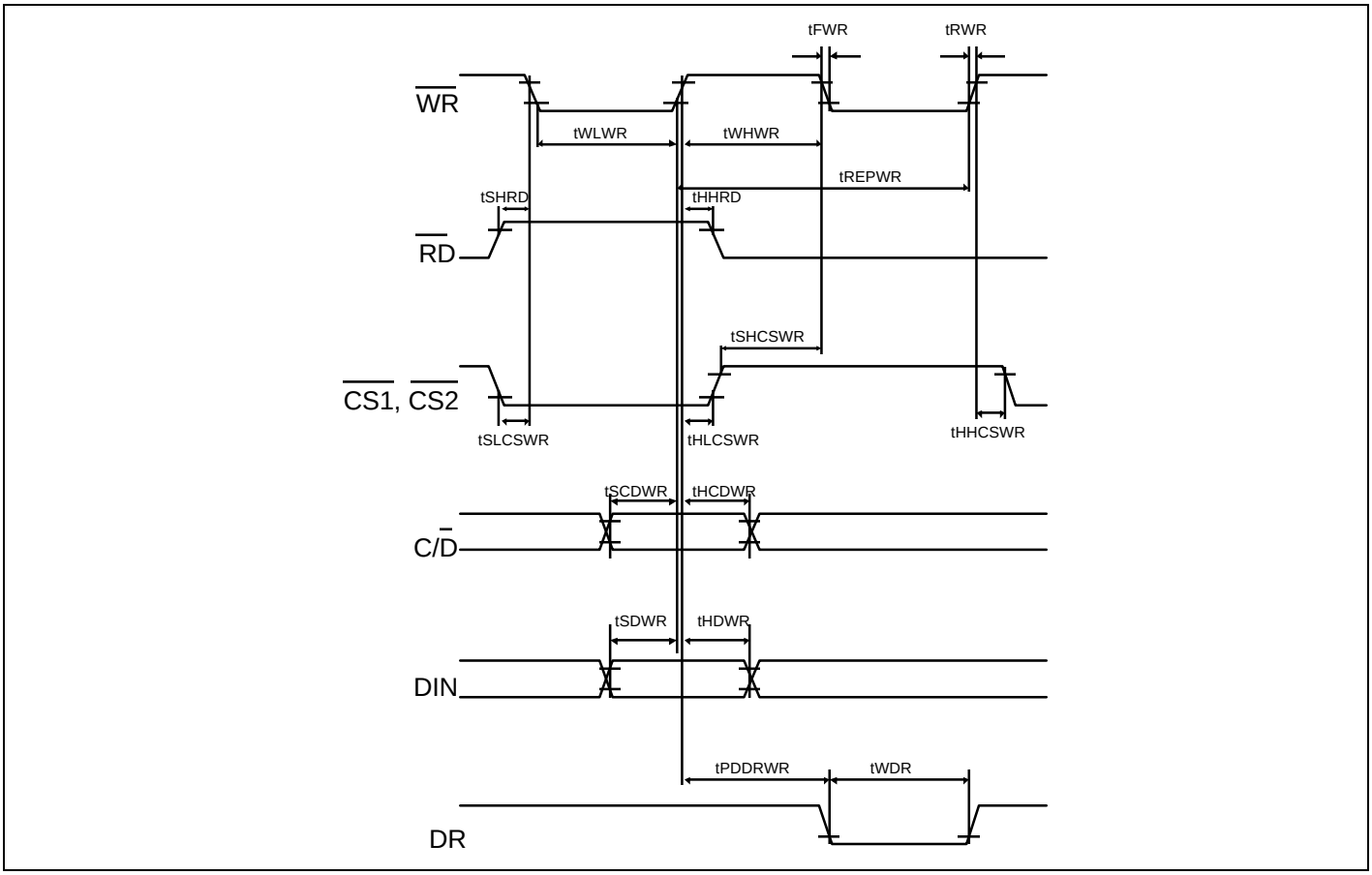


Figure 6 Write Timing

Read Timing Characteristics (Figure 7): Operation over recommended temperature and voltage range

Symbol	Parameter	Condition	Min.	Typ.*	Max.	Units
tWLRD	Read Pulse Low Width		180			ns
tWHRD	Read Pulse High Width		tCK			ns
tREPRD	Repetition Interval between active Read Pulses	tREP=40+2 tCK+tWLCK + tRCK		see formula		ns
tSHRD	High Level Setup Time to active Write Pulse		0			ns
tHHRD	High Level Hold Time from active Write Pulse		20			ns
tRWR	Read Pulse Rise Time				60	ns
tFWR	Read Pulse Fall Time				60	ns
tSLCSRD	CS Low Setup Time to RD Falling Edge	Active State	0			ns
tHCSRD	CS Low Hold Time from RD Rising Edge	Active State	0			ns
tSHCSRD	CS High Setup Time to RD Falling Edge	Inactive State	0			ns
tHHCSRD	CS High Hold Time from RD Rising Edge	Inactive State	0			ns

Read Timing Characteristics (Continued): Operation over recommended temperature and voltage range

Symbol	Parameter	Condition	Min.	Typ.*	Max.	Units
tSCDRD	C/D Setup Time to Read Pulse Start		20			ns
tHCDRD	C/D Hold Time from Read PulseEnd		25			ns
tSASRD	Address Select Setup Time to Read Pulse Start		20			ns
tHASRD	Address Select Hold Time from Read Pulse End		25			ns
tPDD	Data Delay Time	CL = 200pF			120	ns
tHZ	Delay Time to High Z				80	ns

Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing

Note: Because of internal clock re-synchronization, one single additional requirement is recommended in order to produce a simultaneous instruction flow in a multi-chip configuration: The RD rising edge has to be 20 to 20 + tWL(CK) ns late relative to clock falling edge.

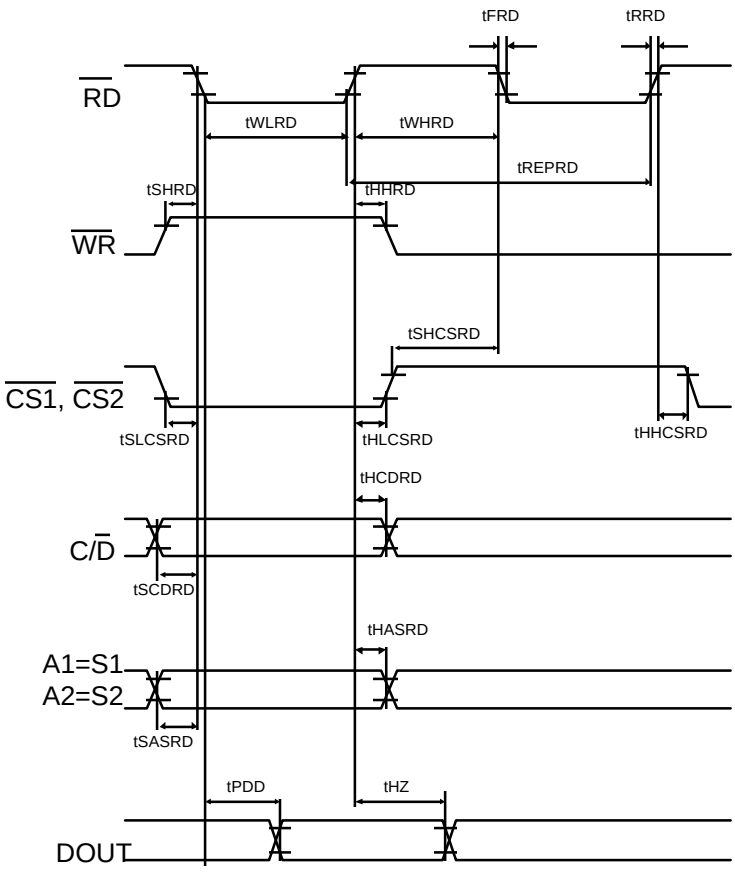


Figure 7 Read Timing

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