

### Typical Applications

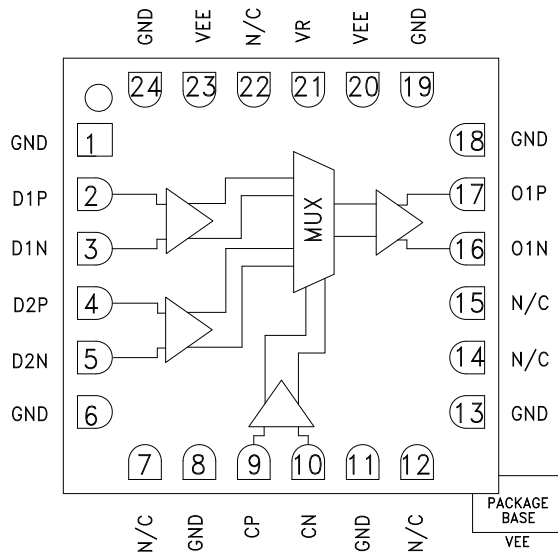
The HMC954LC4B is ideal for:

- SONET OC-192
- Broadband Test & Measurement Equipment
- FPGA Interfacing Circuitry
- 16 G and 32 G Fiber Channel
- 100 Gbit Ethernet

### Features

- Supports Data Rates up to 32 Gbps
- 479 mW Power Consumption
- -3.3 V or +3.3 V Operation is Available
- Supports Single-Ended and Differential Operation
- 24 Lead Ceramic 4x4 mm SMT Package: 16 mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC954LC4B is a 2 to 1 Multiplexer designed for 32 Gbps data serialization. The mux latches the two differential inputs on a rising edge of the input clock. The device uses both rising and falling edges of the half-rate clock to serialize the data. The HMC954LC4B also features an output level control pin, VR, which allows for loss compensation or for signal-level optimization.

All differential inputs to the HMC954LC4B are CML and terminated on-chip with 50 Ohms to the positive supply, GND, and may be AC or DC coupled. The differential CML outputs are source terminated to 50 Ohms and may also be AC or DC coupled. Outputs can be connected directly to a 50 Ohm ground-terminated system or drive devices with CML logic input. The HMC954LC4B operates from a single -3.3 V supply and is available in a ceramic ROHS-compliant 4x4 mm SMT package.

### Electrical Specifications, $T_A = +25\text{ }^\circ\text{C}$ , $V_{ee} = -3.3\text{ V}$ , $VR = 0\text{ V}$

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage (Vee)		-3.6	-3.3	-3.0	V
Power Supply Current			145		mA
Maximum Output Data Rate			32		Gbps
Maximum Clock Rate			16		GHz
Input Voltage Range, C and DIN		-1.5		0.5	V
Input Differential Range, C and DIN		0.1		2.0	Vp-p
Data Input Return Loss	Frequency <24 Gbps		10		dB
Clock Input Return Loss	Frequency <16 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		640		mVp-p
	Differential, peak-to-peak		1280		mVp-p
Output High Voltage			-20		mV
Output Low Voltage			-660		mV

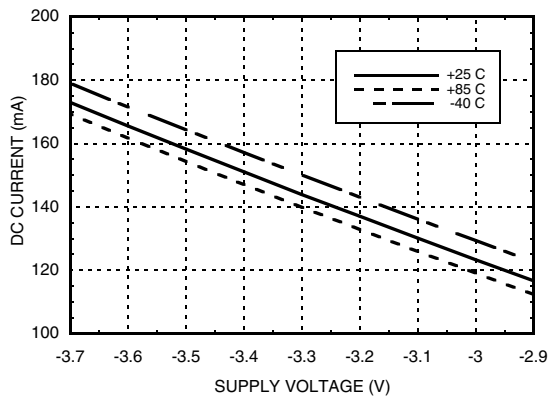


### Electrical Specifications (continued)

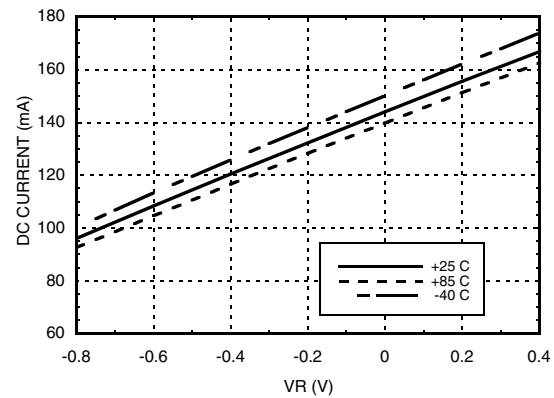
Parameter	Conditions	Min.	Typ.	Max.	Units
Output Rise / Fall Time	Single-Ended, 20% - 80%		15		ps
Output Return Loss	Frequency <28 Gbps		10		dB
Random Jitter $J_R$	rms <sup>[1]</sup>		<0.2		ps rms
VR Pin Current	VR = 0.0 V		5		mA
Deterministic Jitter, $J_D$	$\delta - \delta$ , 2 <sup>7</sup> -1 PRBS input <sup>[1]</sup>		<2		ps
Propagation Delay, t <sub>cpd</sub>	Falling Edge		113		ps
Data Setup Time, t <sub>s</sub>			0		ps
Data Hold Time, t <sub>h</sub>			22		ps

[1] Jitter captured at 13 Gbps, 2<sup>7</sup>-1 PRBS input.

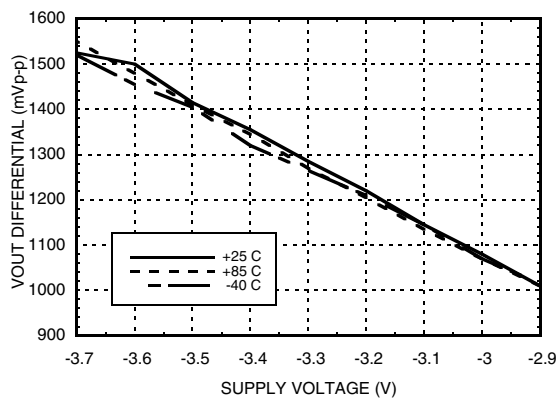
**DC Current vs. Supply Voltage** <sup>[1][2]</sup>



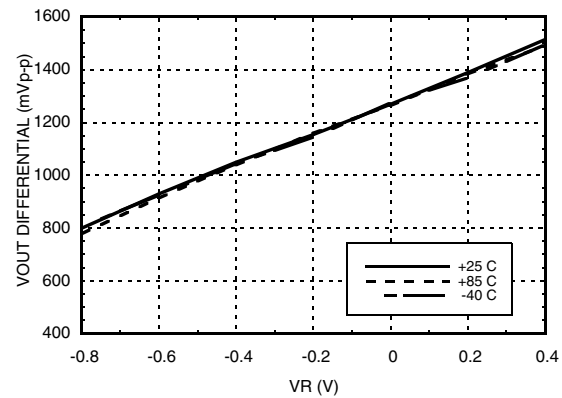
**DC Current vs. VR** <sup>[2][3]</sup>



**Data Output Differential vs. Supply Voltage** <sup>[1][2]</sup>



**Data Output Differential vs. VR** <sup>[2][3]</sup>

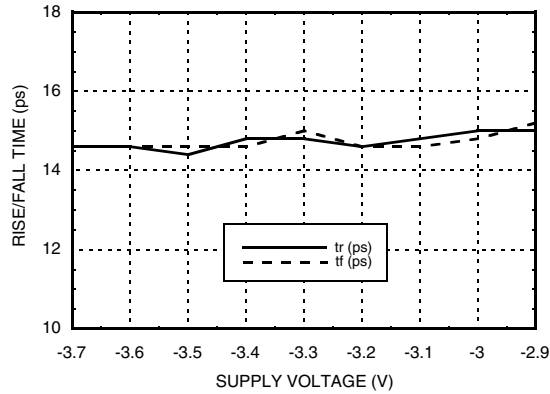


[1] VR = 0.0 V

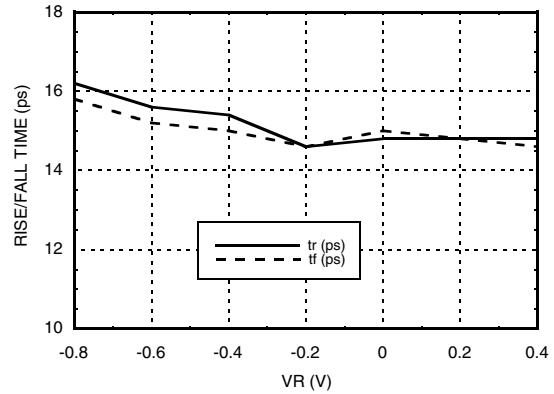
[2] Frequency = 32 Gbps

[3] Vee = -3.3 V

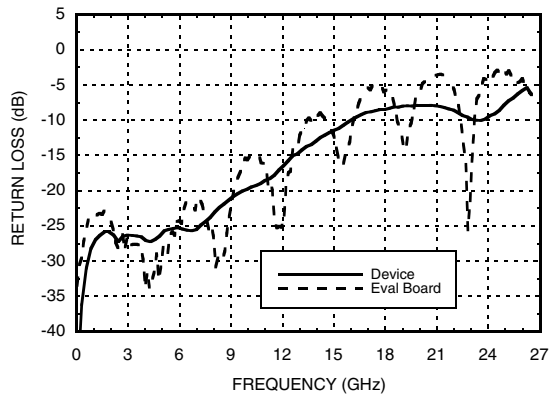
**Rise / Fall Time vs. Supply Voltage [1][2]**



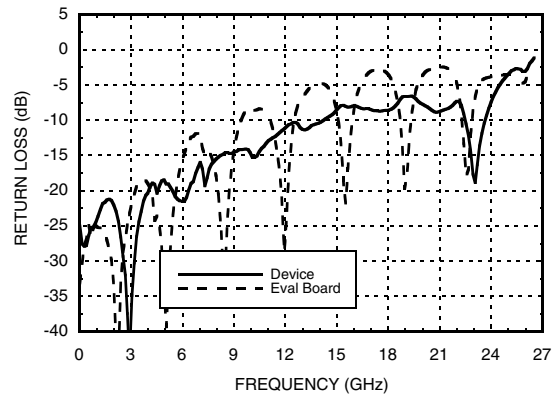
**Rise / Fall Time vs. VR [2][4]**



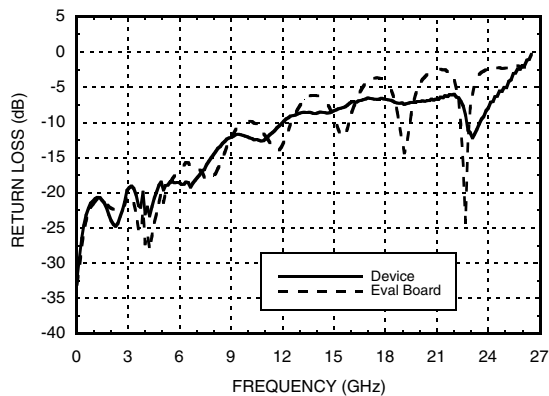
**Clock Input Return Loss vs. Frequency [1][3][4]**



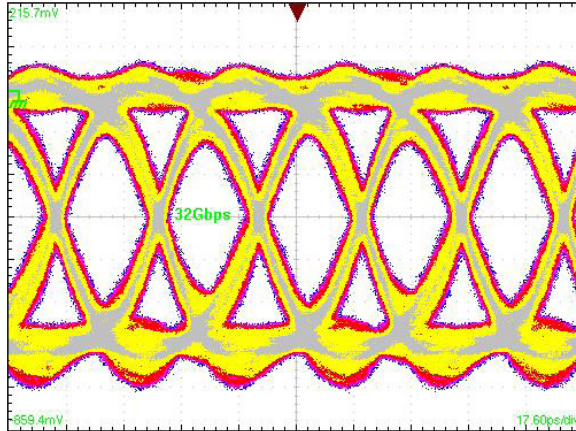
**Data Output Return Loss vs. Frequency [1][3][4]**



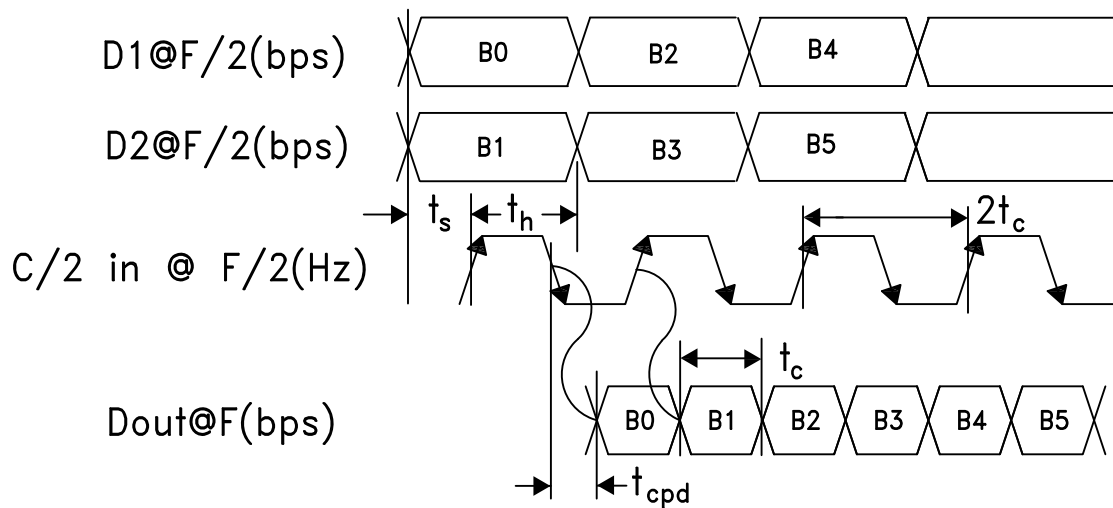
**Data Input Return Loss vs. Frequency [1][3][4]**



[1] VR = 0.0 V      [2] Frequency = 32 Gbps      [3] Device measured on evaluation board with gating after connector  
 [4] Vee = -3.3 V

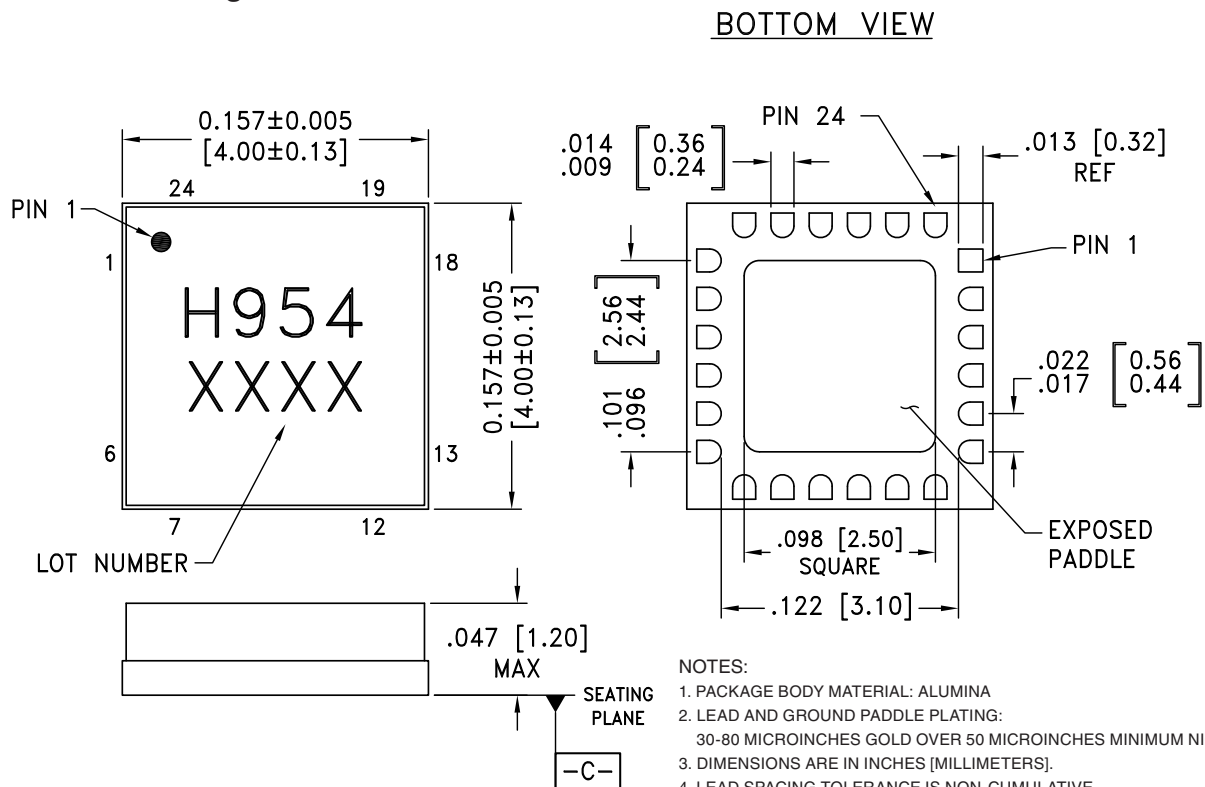
**Eye Diagram, 32 Gbps**


[1] Test Conditions:  
 Single-ended 200 mV, 16 Gbps data input; 16 GHz clock input  
 Pattern generated with a  $2^7-1$  PN, 16 Gbps PRBS pattern  
 Resulting in a Quasi PN 32 Gbps output measured with Tektronix  
 CSA 8000

**Timing Diagram**


**Absolute Maximum Ratings**

Power Supply Voltage (Vee)	-3.75 V to +0.5 V
Input Signals	-2 V to +0.5 V
Output Signals	-1.5 V to +1 V
Junction Temperature	125 °C
Continuous Pdiss (T=85 °C) (derate 30 mW/°C above 85 °C)	1.22 W
Thermal Resistance (R <sub>th j-p</sub> ) Worse case junction to package paddle	32.8 °C/W
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1C


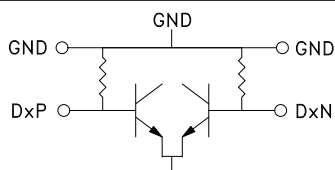
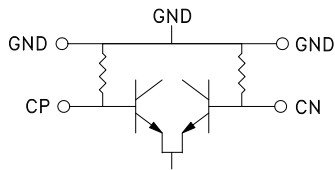
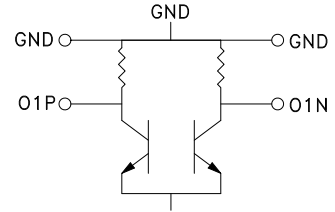

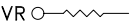

**ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS**
**Outline Drawing**

**Package Information**

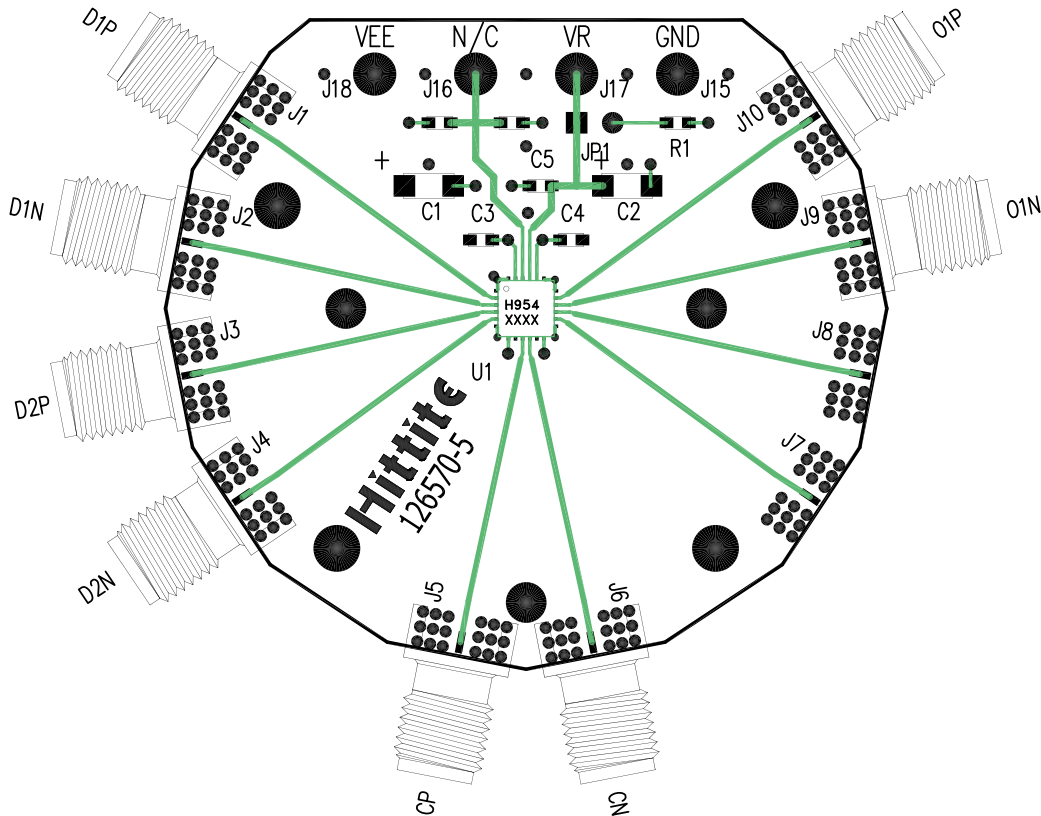
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking <sup>[2]</sup>
HMC954LC4B	Alumina, White	Gold over Nickel	MSL3 <sup>[1]</sup>	H954 XXXX

[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX

**Pin Descriptions**

Pin Number	Function	Description	Interface Schematic
1, 6, 8, 11, 13, 18	GND	Signal Grounds	
2, 3 4, 5	D1P, D1N D2P, D2N	Differential Data Inputs: Current Mode Logic (CML) referenced to positive supply.	
7, 12, 14, 15, 22	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
9, 10	CP, CN	Differential Clock Inputs: Current Mode Logic (CML) referenced to positive supply.	
16, 17	O1N, O1P	Differential Outputs: Current Mode Logic (CML) referenced to positive supply	
19, 24	GND	Supply Grounds	
20, 23 Package Base	Vee	These pins and the exposed paddle must be connected to the negative voltage supply.	
21	VR	Output level control. Output level may be increased or decreased by applying a voltage to VR per "Output Differential vs. VR" plot.	

**Evaluation PCB**

**List of Materials for  
Evaluation PCB EVAL01-HMC954LC4B [1]**

Item	Description
J1 - J6, J9, J10	PCB Mount 2.92 mm RF Connectors
J15 - J18	DC Pin
JP1	0.1" Header with Shorting Jumper
C1, C2	4.7 $\mu$ F Capacitor, Tantalum
C3 - C5	330 pF, Capacitor, 0603 Pkg
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC954LC4B High Speed Logic, 2:1 Mux
PCB [2]	126570 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

**Application Circuit**
