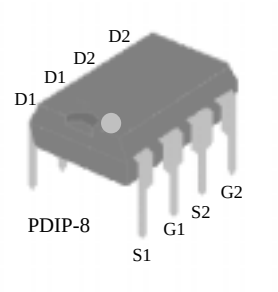
Advanced Power Electronics Corp.

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

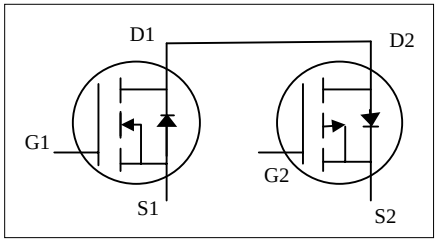
- ▼ **Simple Drive Requirement**
- ▼ **Low On-resistance**
- ▼ **Fast Switching**



N-CH	BV_{DSS}	20V
	$R_{DS(ON)}$	60mΩ
	I_D	2.6A
P-CH	BV_{DSS}	-20V
	$R_{DS(ON)}$	80mΩ
	I_D	-2.3A

Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	±12	±12	V
I_D@T_A=25℃	Continuous Drain Current[3]	2.6	-2.3	A
I_D@T_A=70℃	Continuous Drain Current[3]	2.1	-1.8	A
I_{DM}	Pulsed Drain Current[1]	15	-10	A
P_D@T_A=25℃	Total Power Dissipation	2		W
	Linear Derating Factor	0.016		W/℃
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter		Value	Unit
Rthj-a	Thermal Resistance Junction-ambient[3]	Max.	62.5	℃/W

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	20	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25℃, I_D=1mA	-	0.037	-	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=4.5V, I_D=2.6A	-	-	60	mΩ
		V_{GS}=2.5V, I_D=1.8A	-	-	90	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	0.5	-	1.2	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=2.6A	-	3.6	-	S
I_{DSS}	Drain-Source Leakage Current (T_j=25°C)	V_{DS}=20V, V_{GS}=0V	-	-	1	uA
	Drain-Source Leakage Current (T_j=150°C)	V_{DS}=16V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±12V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=2.6A	-	9	-	nC
Q_{gs}	Gate-Source Charge	V_{DS}=10V	-	1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	4	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=10V	-	6.5	-	ns
t_r	Rise Time	I_D=1A	-	14	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=6Ω,V_{GS}=4.5V	-	20	-	ns
t_f	Fall Time	R_D=10Ω	-	15	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	300	-	pF
C_{oss}	Output Capacitance	V_{DS}=8V	-	255	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	115	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	V_D=V_G=0V , V_S=1.2V	-	-	1.7	A
V_{SD}	Forward On Voltage[2]	T_j=25℃, I_S=1.7A, V_{GS}=0V	-	-	1.2	V

P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	-20	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25℃, I_D=-1mA	-	-0.037	-	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-4.5V, I_D=-2.2A	-	-	80	mΩ
		V_{GS}=-2.5V, I_D=-1.8A	-	-	135	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-0.5	-	-1	V
g_{fs}	Forward Transconductance	V_{DS}=-5V, I_D=-2.2A	-	2.7	-	S
I_{DSS}	Drain-Source Leakage Current (Tj=25°C)	V_{DS}=-20V, V_{GS}=0V	-	-	-1	uA
	Drain-Source Leakage Current (Tj=150°C)	V_{DS}=-16V, V_{GS}=0V	-	-	-25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±12V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=-2.2A	-	11.5	-	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-6V	-	3.2	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-4.5V	-	1.5	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=-10V	-	-	10	ns
t_r	Rise Time	I_D=-2.2A	-	-	25	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=6Ω,V_{GS}=-4.5V	-	-	50	ns
t_f	Fall Time	R_D=4.5Ω	-	-	30	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	940	-	pF
C_{oss}	Output Capacitance	V_{DS}=-15V	-	440	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	130	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	V_D=V_G=0V , V_S=-1.2V	-	-	-1.7	A
V_{SD}	Forward On Voltage[2]	T_j=25℃, I_S=-1.8A, V_{GS}=0V	-	-0.75	-1.2	V

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse width ≤300us , duty cycle ≤2%.

3.Mounted on 1 in^2 copper pad of FR4 board ; 90℃/W when mounted on Min. copper pad.

N-Channel

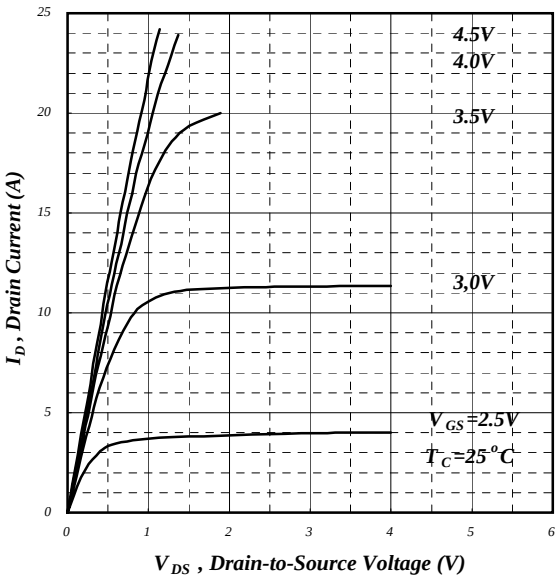


Fig 1. Typical Output Characteristics

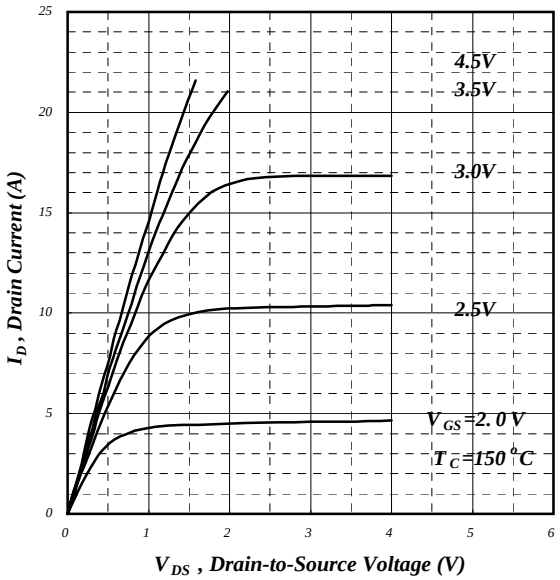


Fig 2. Typical Output Characteristics

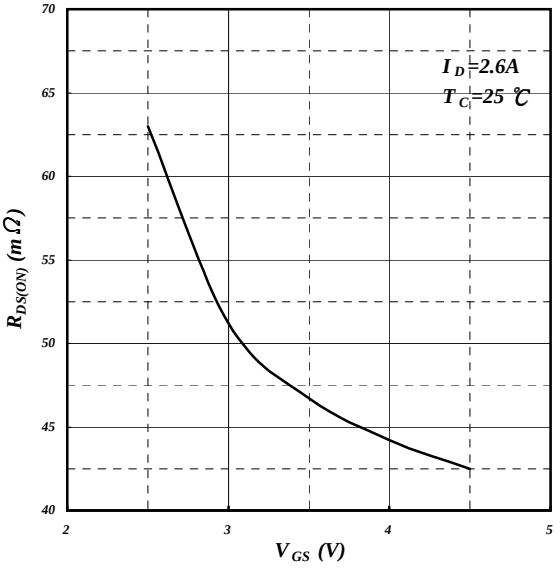


Fig 3. On-Resistance v.s. Gate Voltage

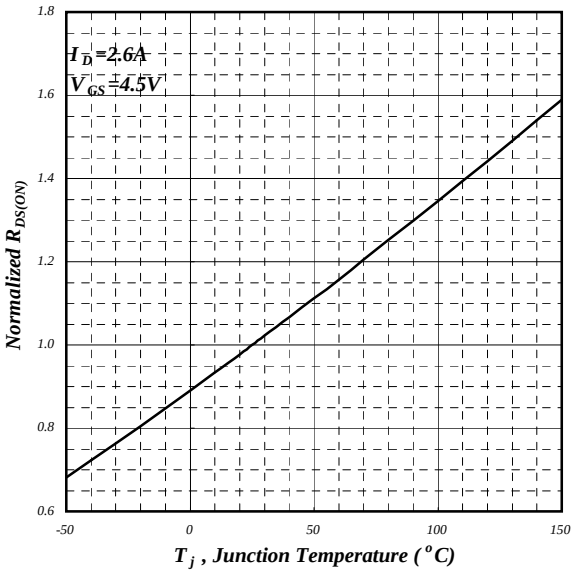


Fig 4. Normalized On-Resistance v.s. Junction Temperature

N-Channel

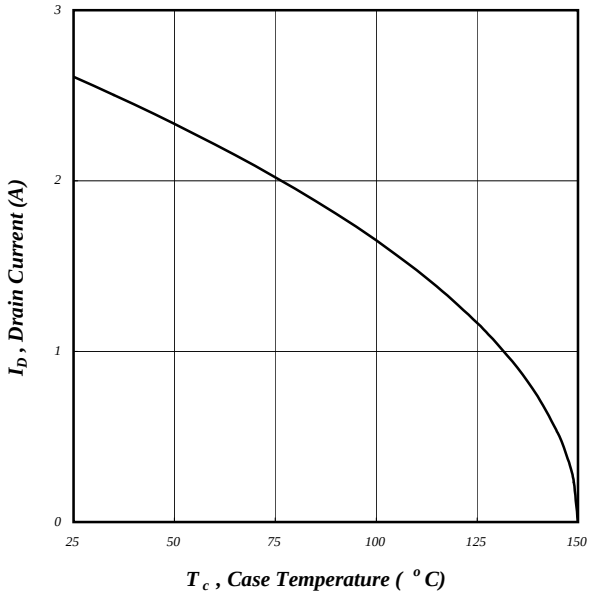


Fig 5. Maximum Drain Current v.s. Case Temperature

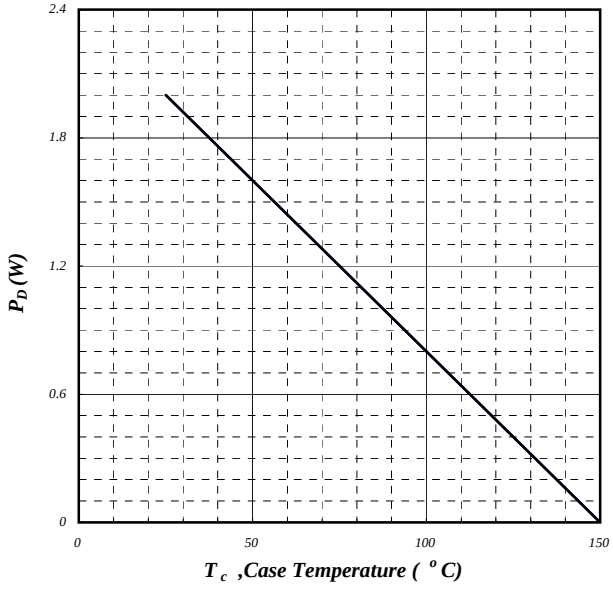


Fig 6. Typical Power Dissipation

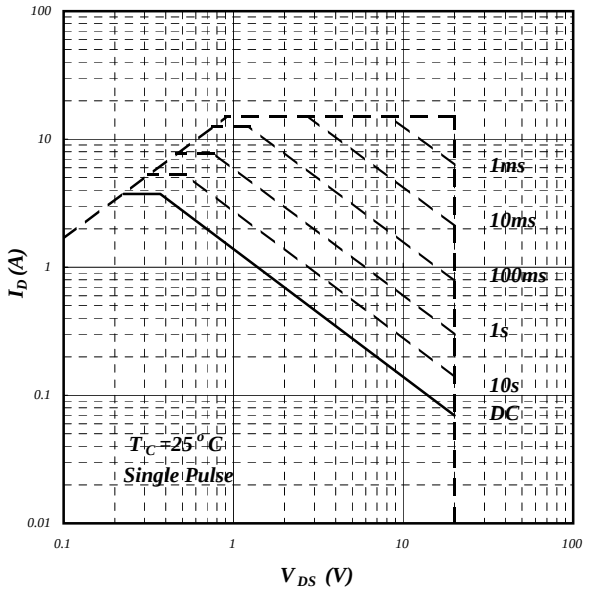


Fig 7. Maximum Safe Operating Area

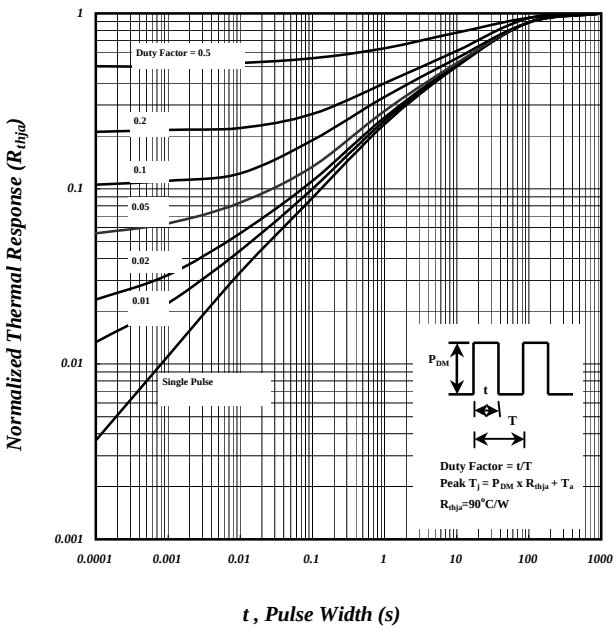


Fig 8. Effective Transient Thermal Impedance

N-Channel

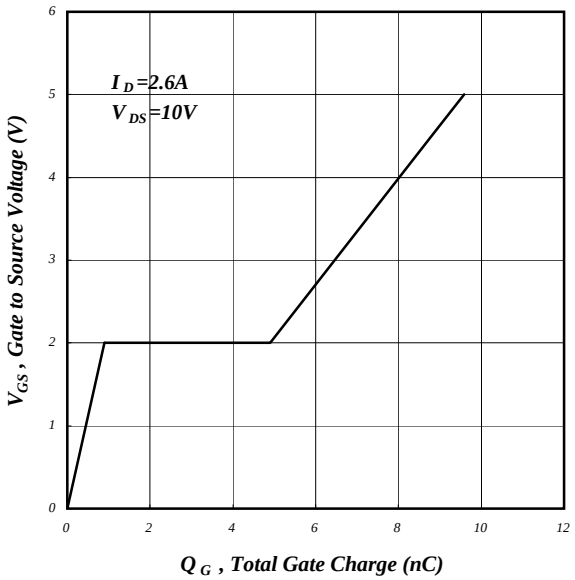


Fig 9. Gate Charge Characteristics

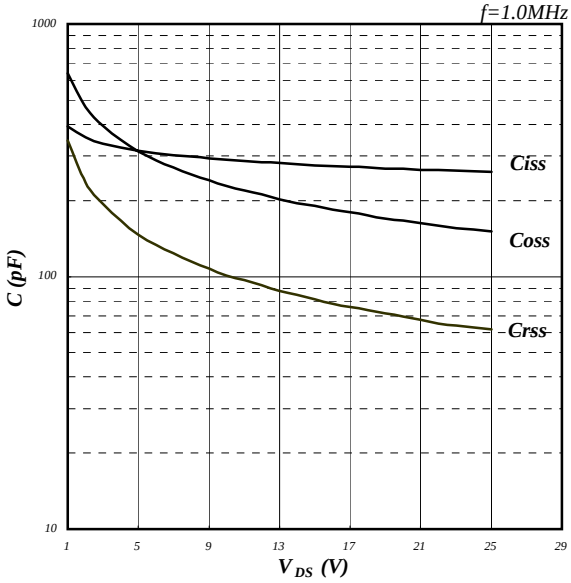


Fig 10. Typical Capacitance Characteristics

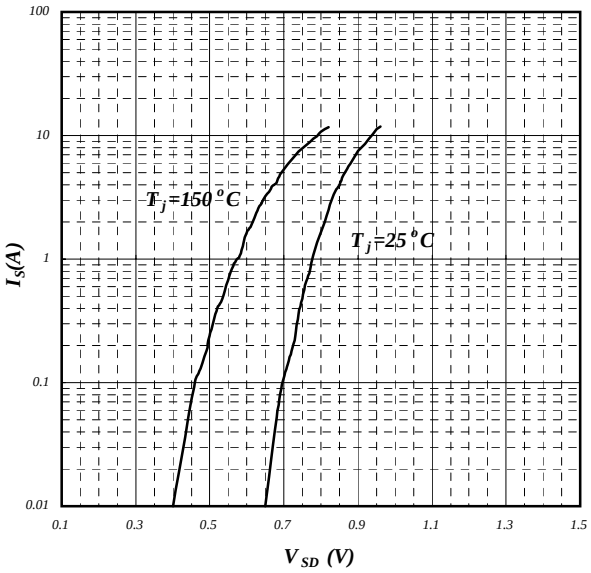


Fig 11. Forward Characteristic of Reverse Diode

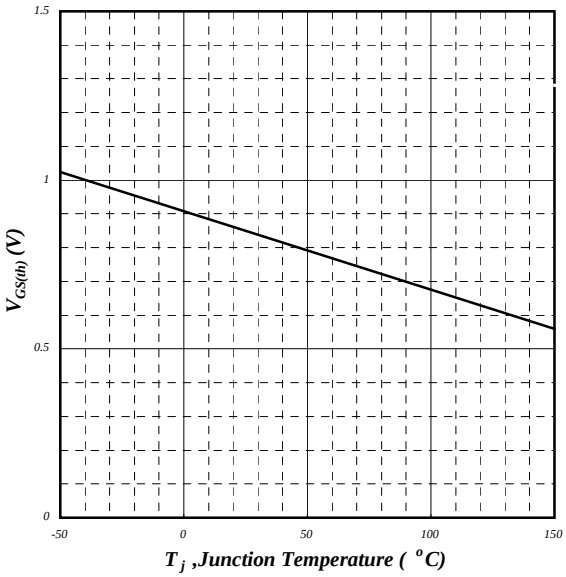


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

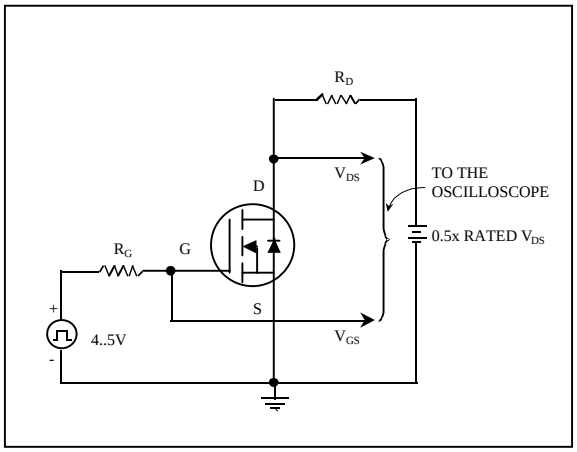


Fig 13. Switching Time Circuit

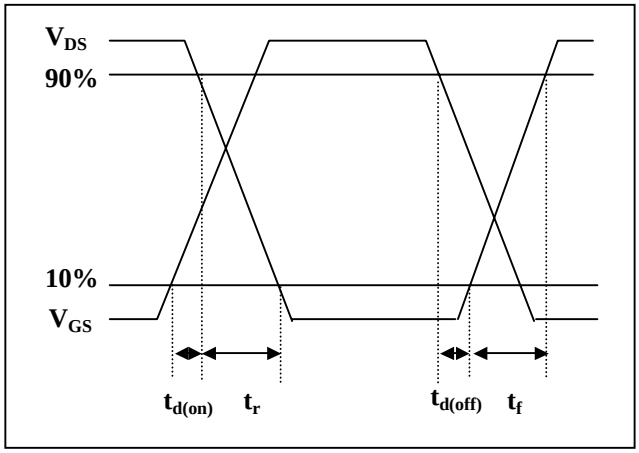


Fig 14. Switching Time Waveform

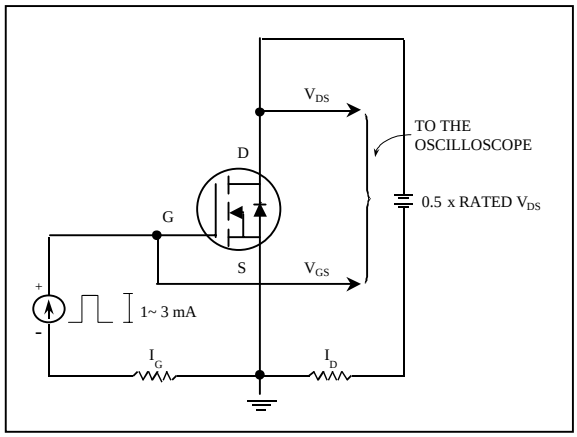


Fig 15. Gate Charge Circuit

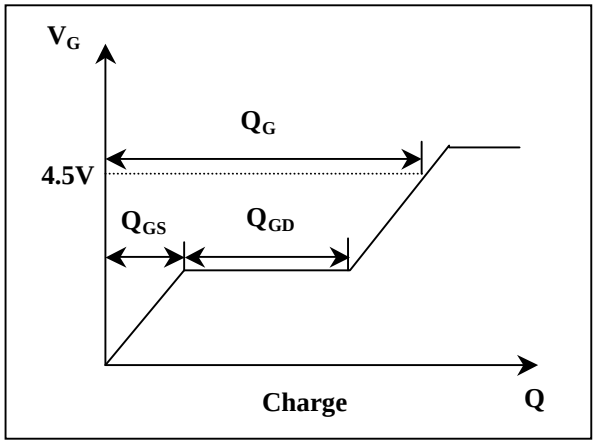


Fig 16. Gate Charge Waveform

P-Channel

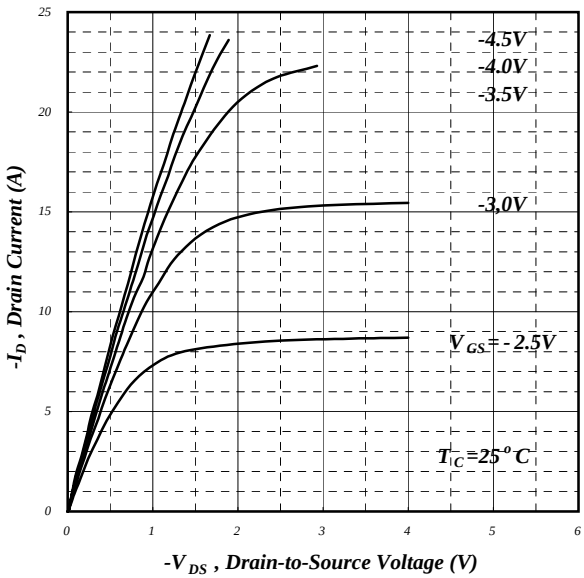


Fig 1. Typical Output Characteristics

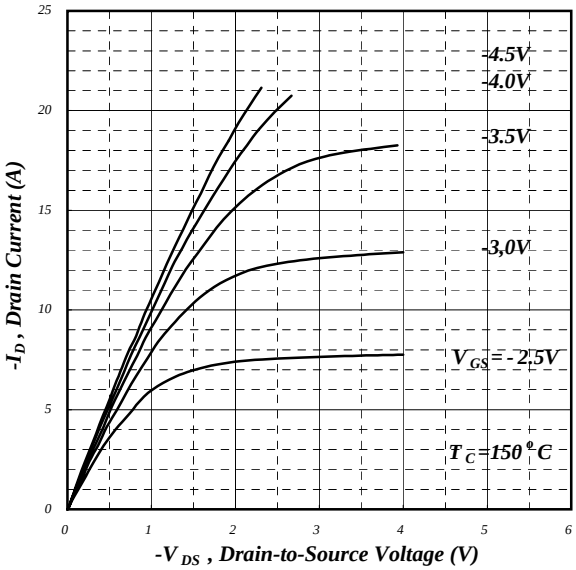


Fig 2. Typical Output Characteristics

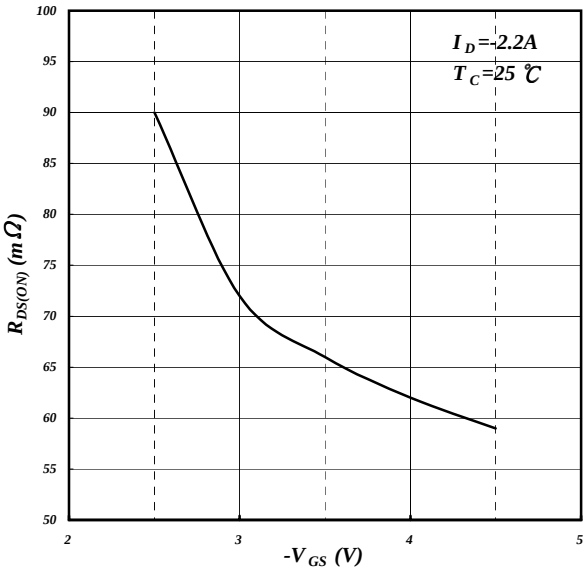


Fig 3. On-Resistance v.s. Gate Voltage

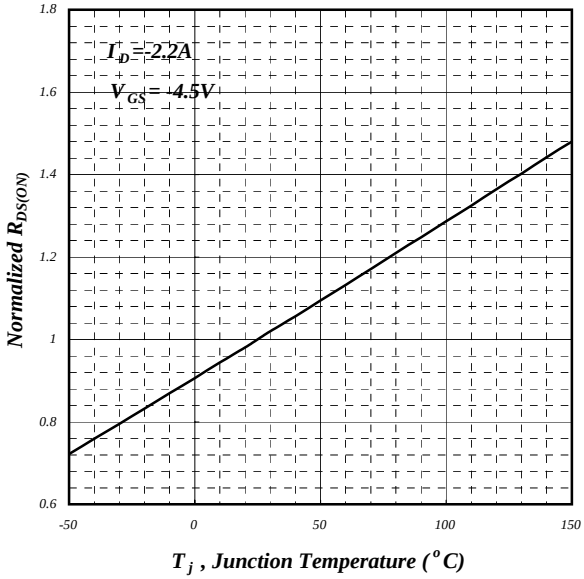


Fig 4. Normalized On-Resistance v.s. Junction Temperature

P-Channel

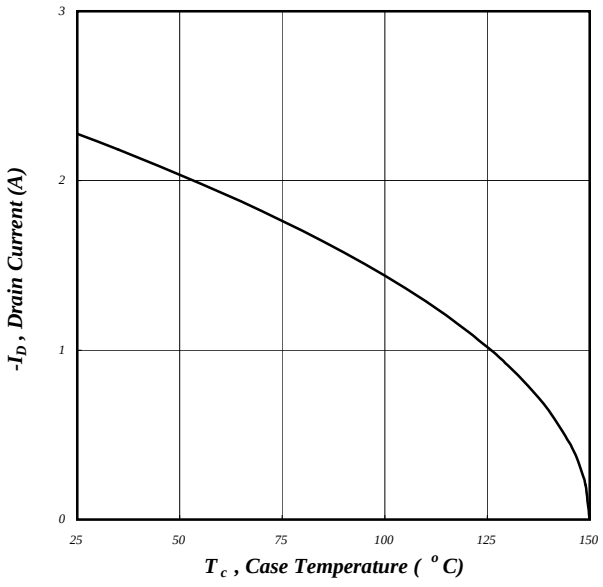


Fig 5. Maximum Drain Current v.s. Case Temperature

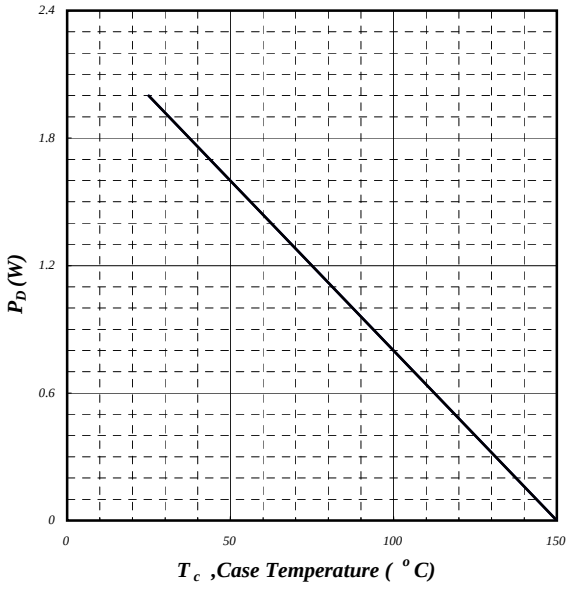


Fig 6. Typical Power Dissipation

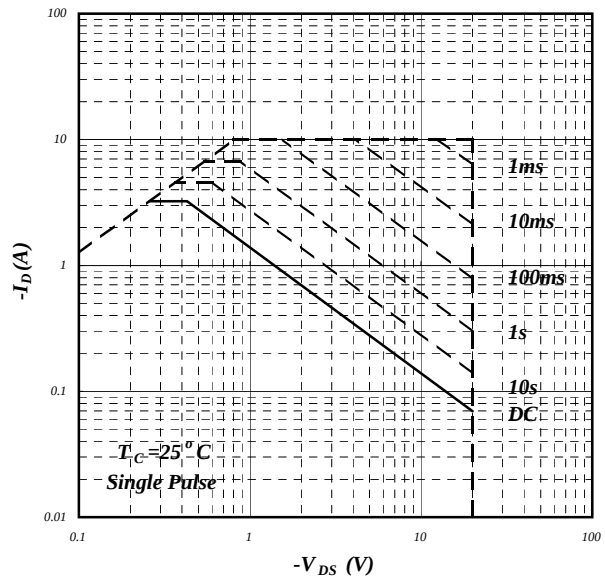


Fig 7. Maximum Safe Operating Area

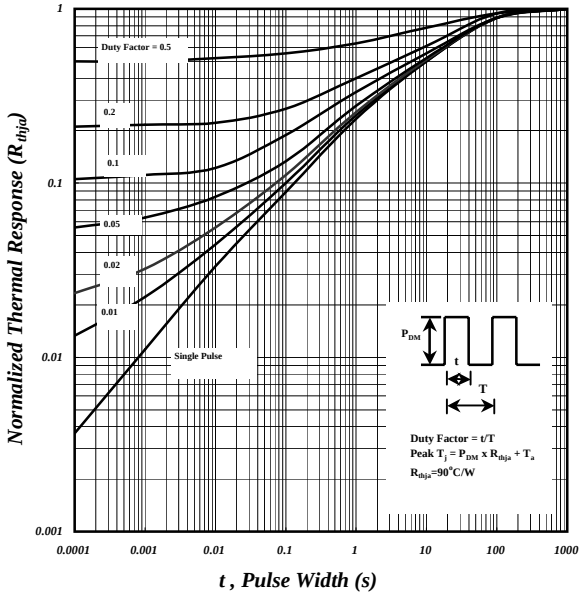


Fig 8. Effective Transient Thermal Impedance

P-Channel

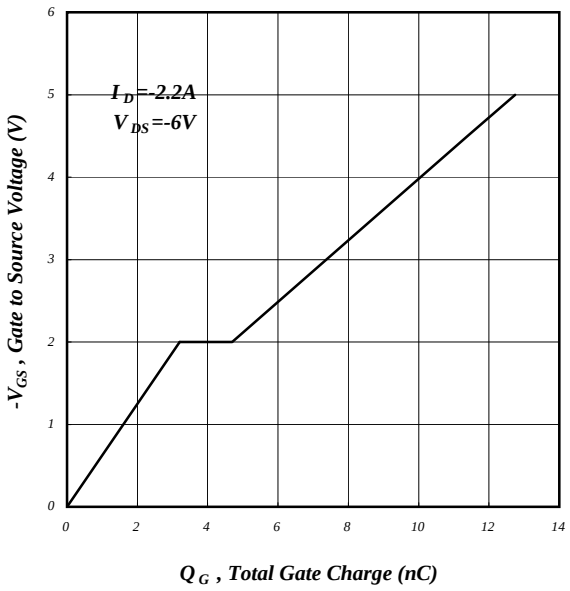


Fig 9. Gate Charge Characteristics

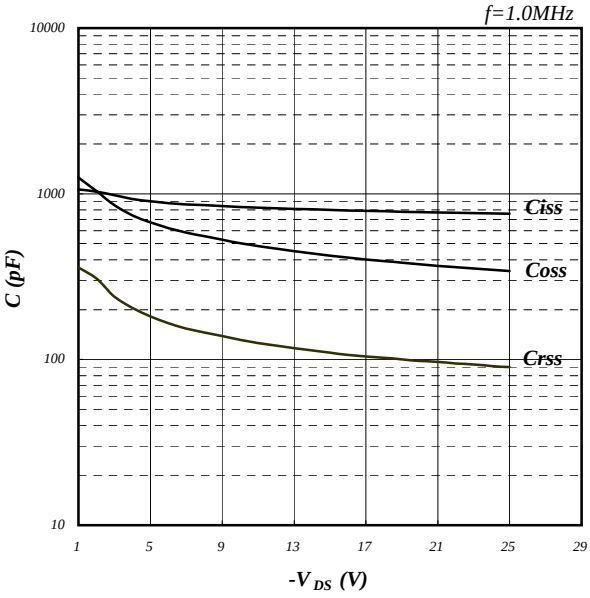


Fig 10. Typical Capacitance Characteristics

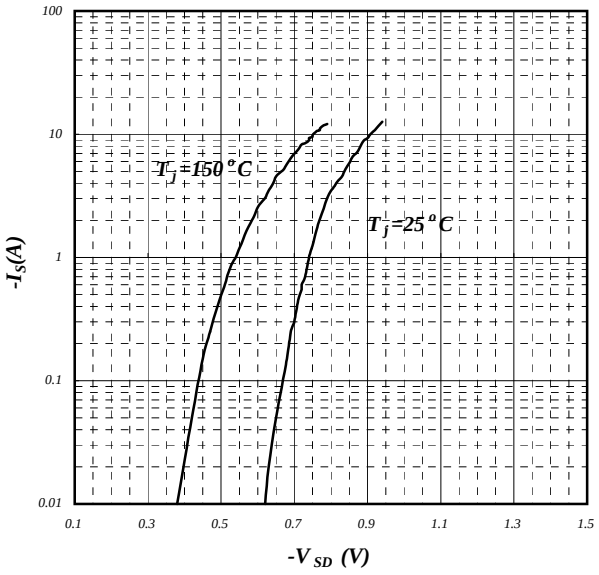


Fig 11. Forward Characteristic of Reverse Diode

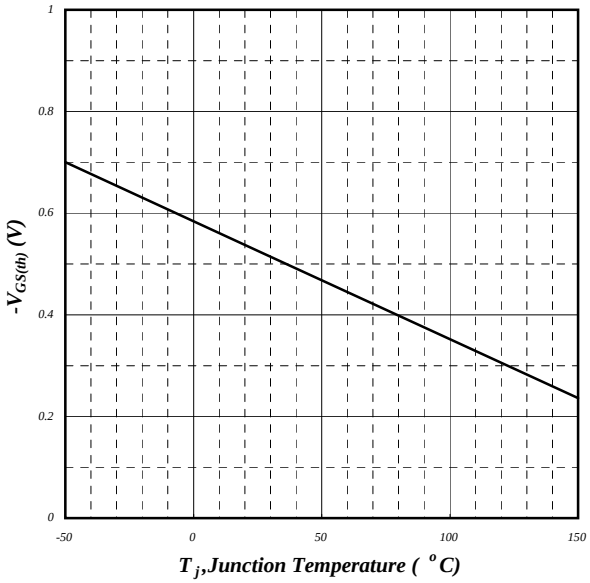


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

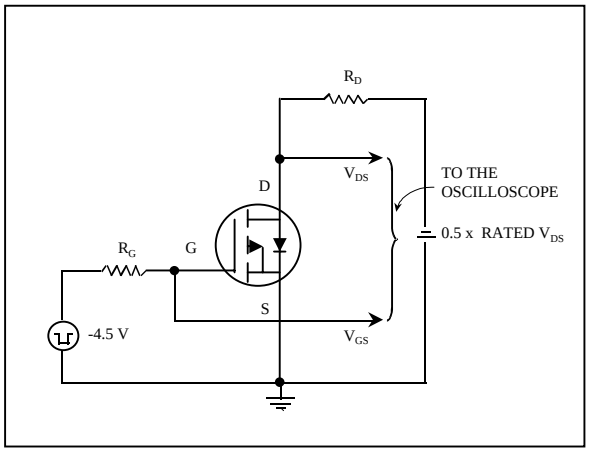


Fig 13. Switching Time Circuit

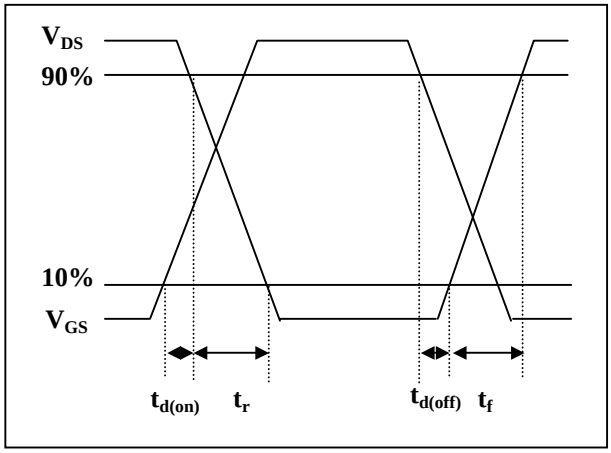


Fig 14. Switching Time Waveform

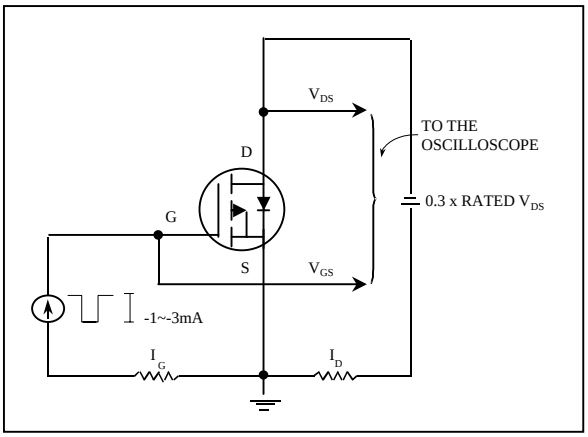


Fig 15. Gate Charge Circuit

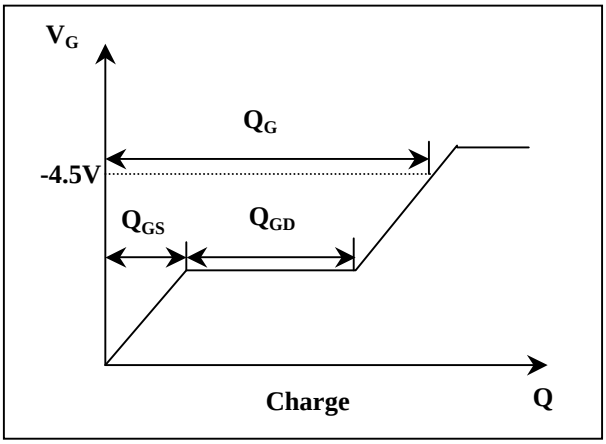


Fig 16. Gate Charge Waveform