

ANSALDO**Ansaldo Trasporti s.p.a.**
Unita' SemiconduttoriVia N. Lorenzi 8 - I 16152 GENOVA - ITALY
Tel. int. +39/(0)10 6556549 - (0)10 6556488
Fax Int. +39/(0)10 6442510
Tx 270318 ANSUSE I -**PHASE CONTROL THYRISTOR****AT847LT**

Repetitive voltage up to **2500 V**
Mean on-state current **3265 A**
Surge current **39.2 kA**

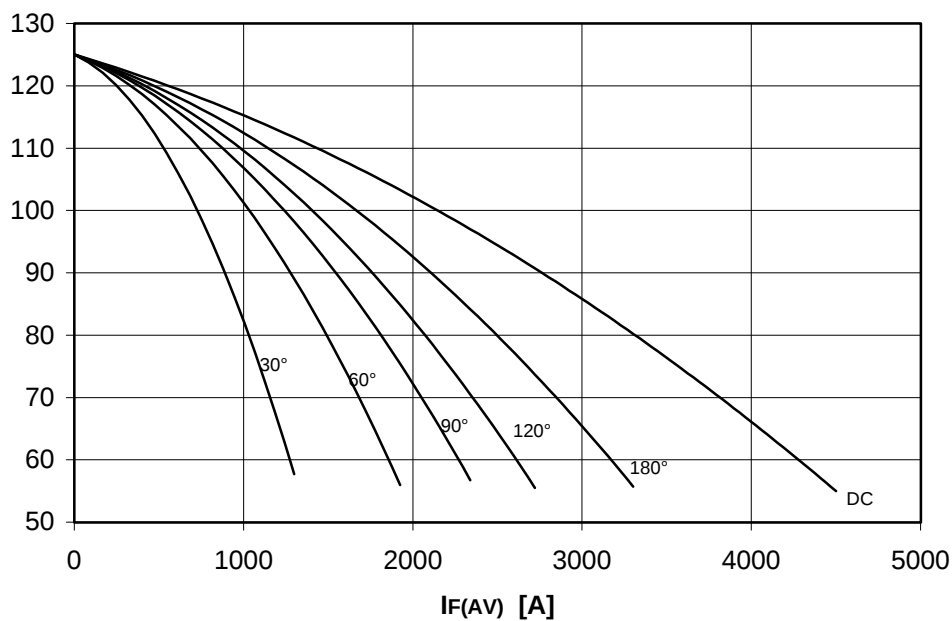
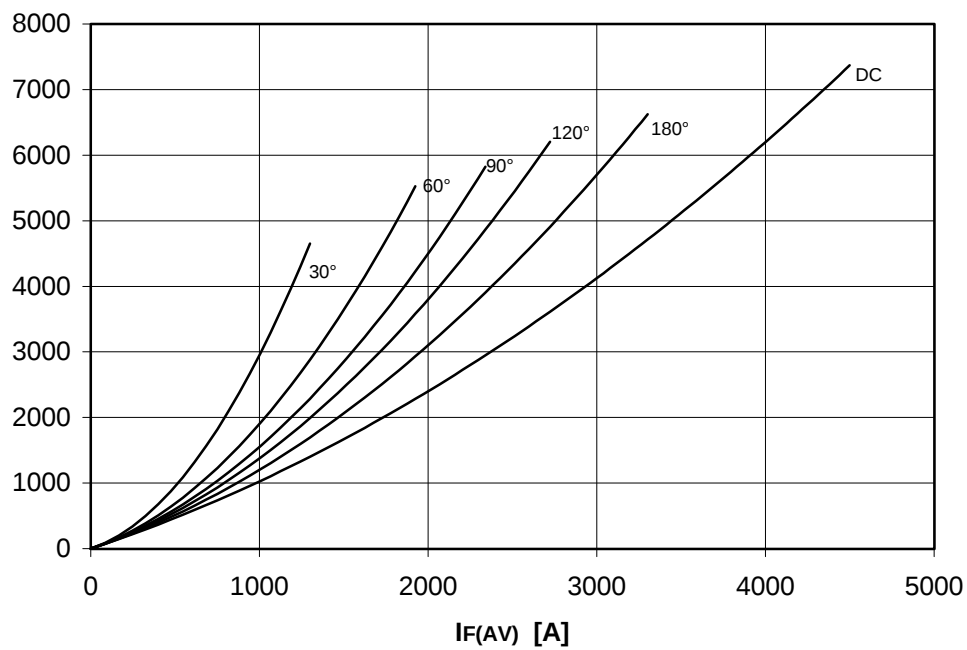
FINAL SPECIFICATION

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Symbol	Characteristic	Conditions	T _j [°C]	Value	Unit
BLOCKING					
V _{RRM}	Repetitive peak reverse voltage		125	2500	V
V _{RSM}	Non-repetitive peak reverse voltage		125	2600	V
V _{DRM}	Repetitive peak off-state voltage		125	2500	V
I _{RRM}	Repetitive peak reverse current	V=V _{RRM}	125	200	mA
I _{DRM}	Repetitive peak off-state current	V=V _{DRM}	125	200	mA
CONDUCTING					
I _{T(AV)}	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		3265	A
I _{T(AV)}	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		2665	A
I _{TSM}	Surge on-state current	sine wave, 10 ms	125	39.2	kA
I ² t	I ² t	without reverse voltage		7683 x1E3	A ² s
V _T	On-state voltage	On-state current = 2100 A	25	1.22	V
V _{T(TO)}	Threshold voltage		125	0.85	V
r _T	On-state slope resistance		125	0.175	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% V _{DRM} up to 3280 A, gate 10V 5ohm	125	800	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of V _{DRM}	125	1000	V/μs
t _d	Gate controlled delay time, typical	VD=100V, gate source 10V, 10 ohm , tr=.5 μs	25	2	μs
t _q	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 75% V _{DRM}	125	400	μs
Q _{rr}	Reverse recovery charge	di/dt=-20 A/μs, I= 2150 A			μC
I _{rr}	Peak reverse recovery current	VR= 50 V			A
I _H	Holding current, typical	VD=5V, gate open circuit	25	500	mA
I _L	Latching current, typical	VD=12V, tp=30μs	25	1000	mA
GATE					
V _{GT}	Gate trigger voltage	VD=12V	25	3.5	V
I _{GT}	Gate trigger current	VD=12V	25	400	mA
V _{GD}	Non-trigger gate voltage, min.	VD=V _{DRM}	125	0.25	V
V _{FGM}	Peak gate voltage (forward)			30	V
I _{FGM}	Peak gate current			10	A
V _{RGM}	Peak gate voltage (reverse)			10	V
P _{GM}	Peak gate power dissipation	Pulse width 100 μs		150	W
P _G	Average gate power dissipation			10	W
MOUNTING					
R _{th(j-h)}	Thermal impedance, DC	Junction to heatsink, double side cooled		9.5	°C/kW
R _{th(c-h)}	Thermal impedance	Case to heatsink, double side cooled		2	°C/kW
T _j	Operating junction temperature			-30 / 125	°C
F	Mounting force			40.0 / 50.0	kN
	Mass			1150	g
ORDERING INFORMATION : AT847LT S 25					
standard specification ☐ VDRM&VRRM/100 ☐					

DISSIPATION CHARACTERISTICS

SQUARE WAVE

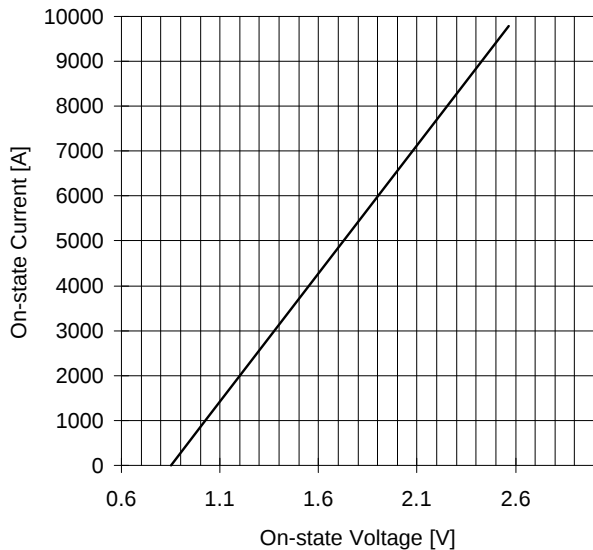
 T_h [°C] $P_F(AV)$ [W]

AT847LT PHASE CONTROL THYRISTOR

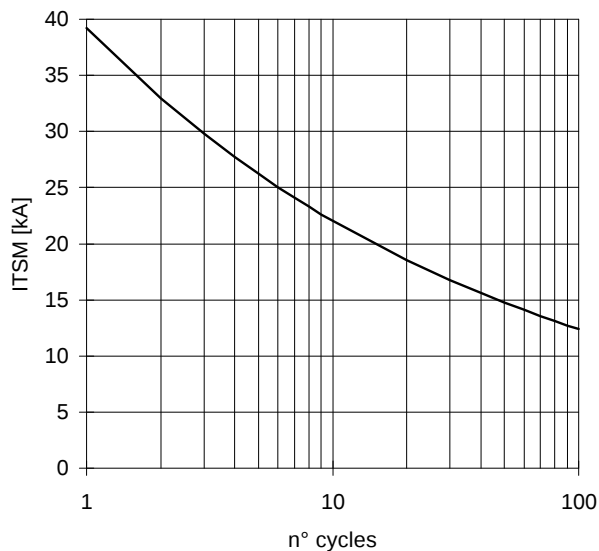
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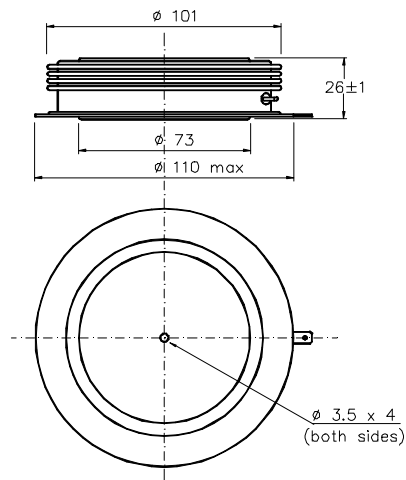
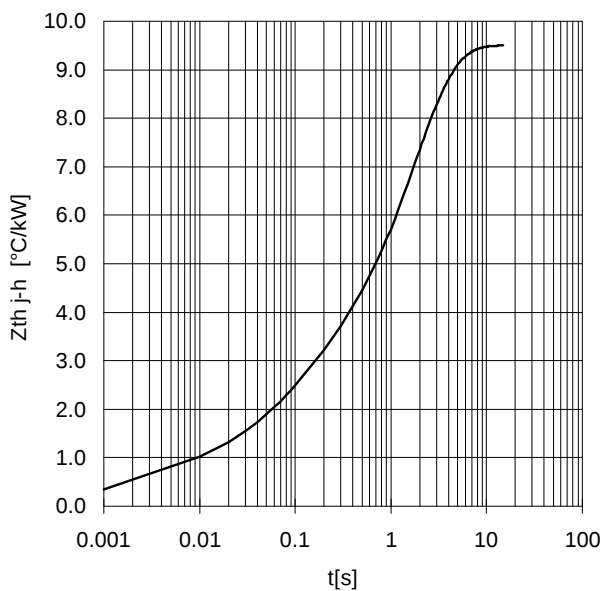
ON-STATE CHARACTERISTIC
 $T_j = 125^\circ\text{C}$



SURGE CHARACTERISTIC
 $T_j = 125^\circ\text{C}$



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED



Dimensions
in mm



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness $< .03$ mm and roughness $< 2 \mu\text{m}$.

In the interest of product improvement ANSALDO reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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