



安森美半导体
ON Semiconductor®

创新型高压集成POL方案 NCP4060/NCP4060A



ON Semiconductor +Fairchild: 更强大

产品

台式机



Vcore 控制器

驱动器

功率级

POL

USB type
C/PD

笔电/ 超薄本/ 2合1



Vcore控制器

驱动器

功率级

POL

电池充电器

USB type
C/PD

无线充电

工业, 电信及 服务器



Vcore控制器

驱动器

POL

功率级

外设, 图 像游戏



GPU控制器

驱动器

功率级

PMIC

POL

无线充电

物联网/ 便携设备



PMIC

无线充电

Vcore控制器

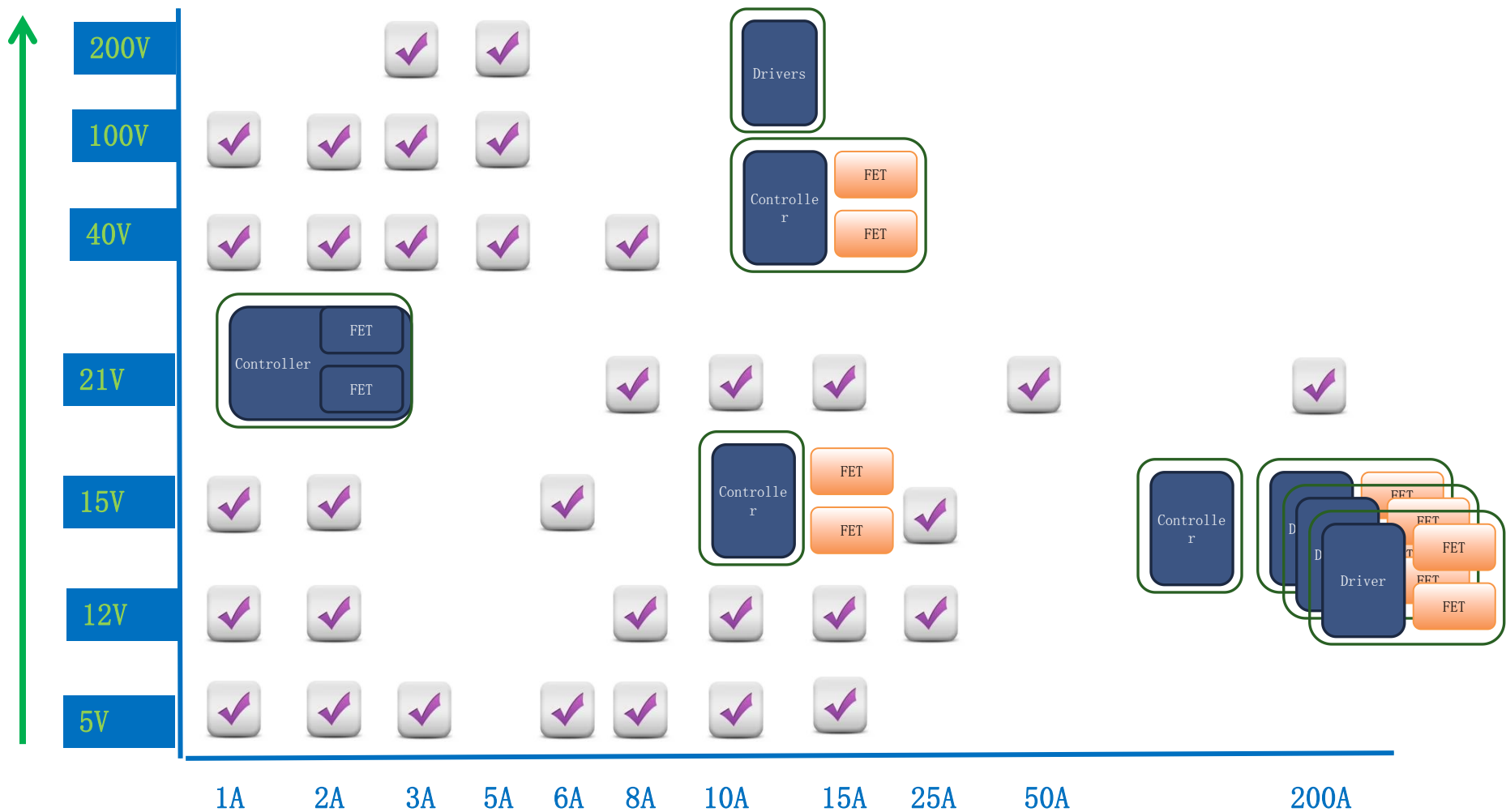
汽车



PMIC

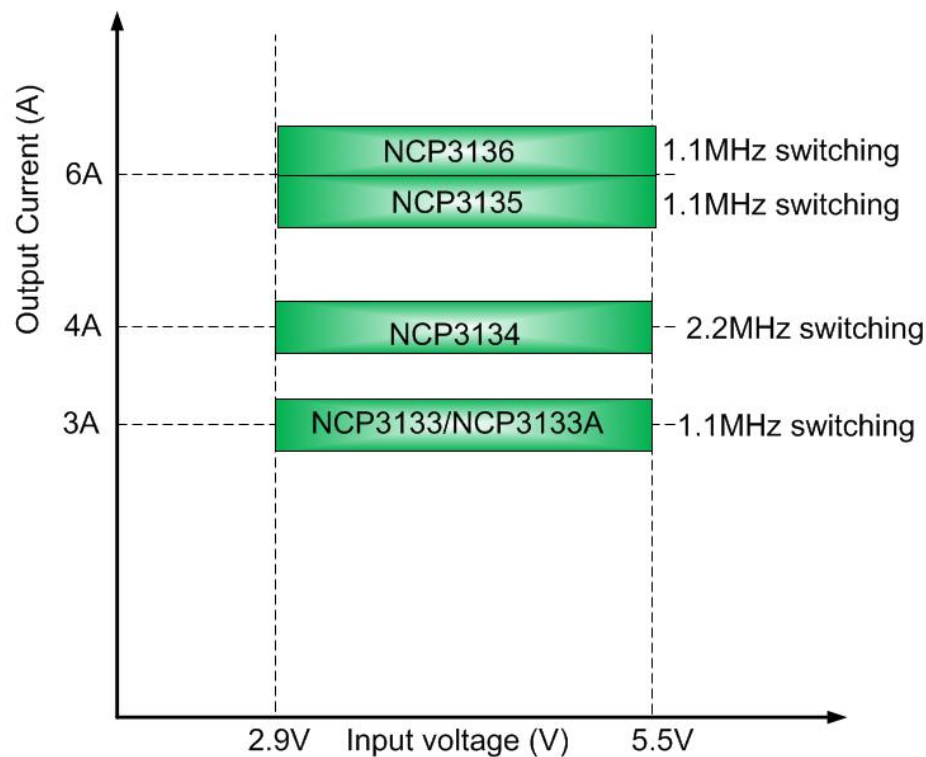
无线充电

完整的阵容



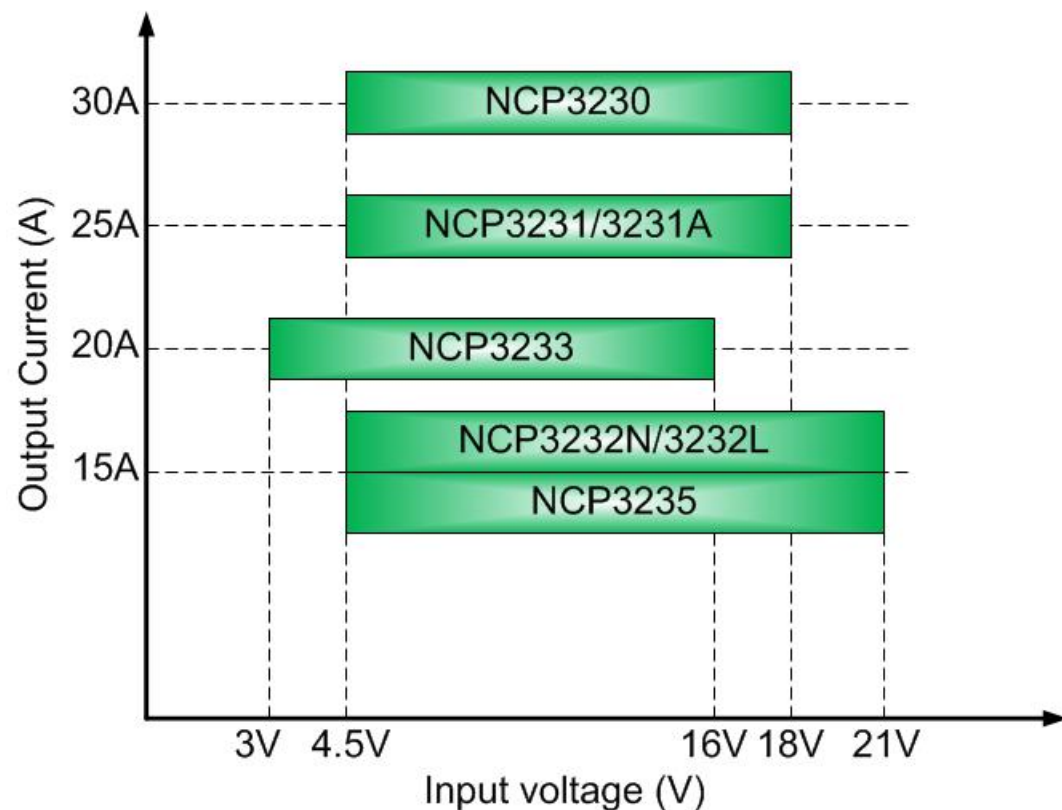
降压稳压器: $V_{IN} \leq 5.5V$

- 此系列共有6个器件



大电流降压稳压器系统

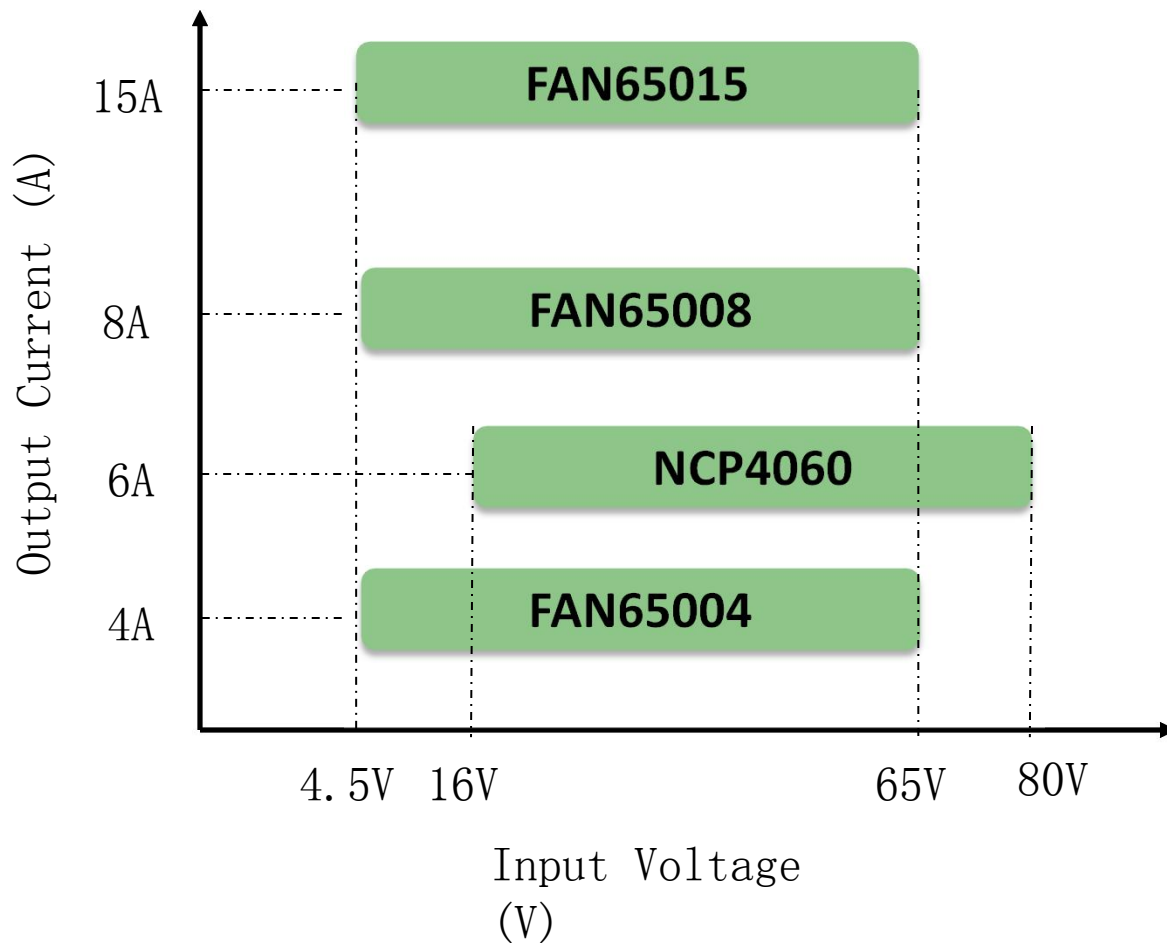
- 此系列共有7个器件



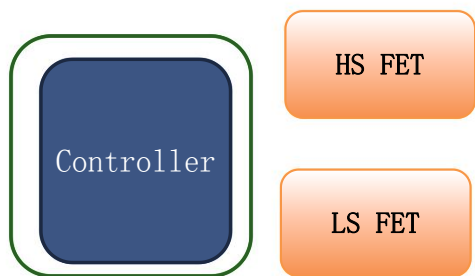
- *NCP3235 轻负载时可工作在非连续导通模式 (DCM) 以改善能效
- *其他器件于整个负载模围内强迫连续导通模式 (FCCM)

高电压降压稳压器系列

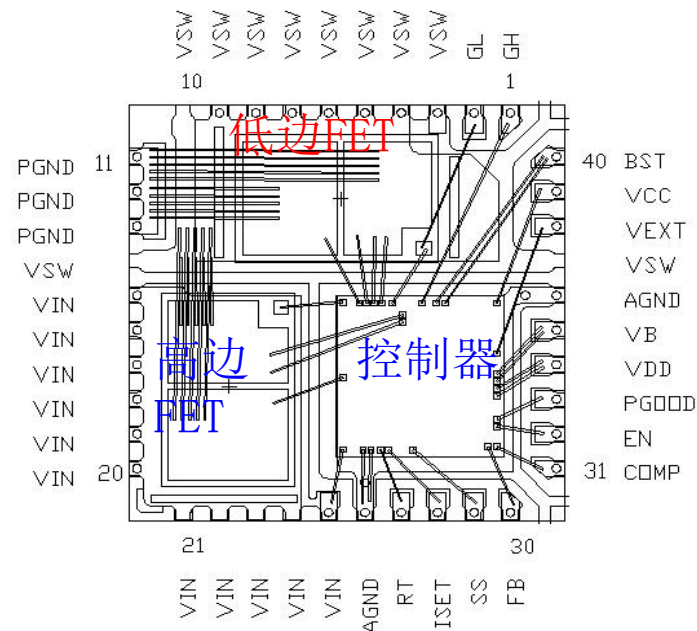
- ON + Fairchild的高压集成POL



NCP4060: 创新型集成稳压器



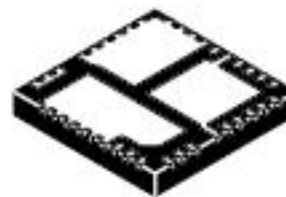
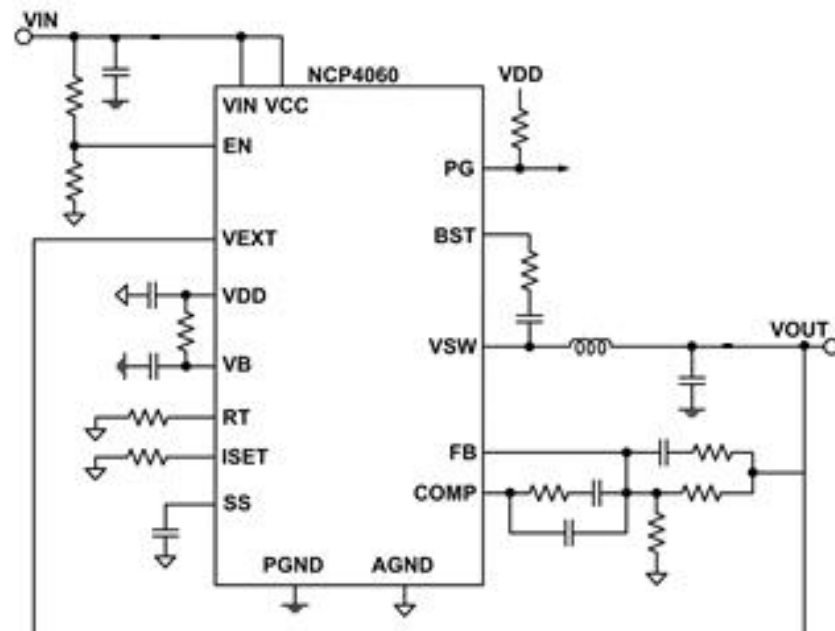
现时的主流器件



ON 创新方案

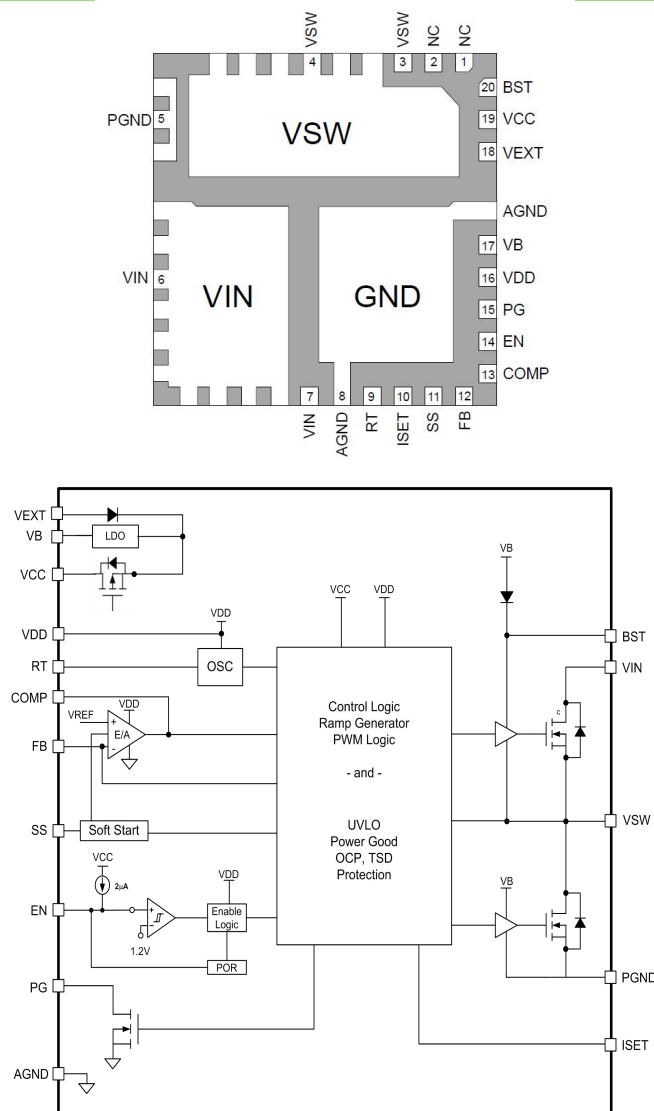
主要特点

- 6x6, 20-引脚 QFN 封装
- 整合 100V 安森美半导体逻辑 FETS，用于高边及低边
- VIN 范围: 16V – 80V
- 高达 6A 连续输出电流 (10A 峰值)
- 可编程开关频率 100kHz~500kHz
- 可编程软启动
- 集成LDO 开关以提高能效
- 无损高边及低边FET电流检测
- Hiccup 保护模式
- 输入电压前馈的电压模式控制



QFN20
CASE 485FC

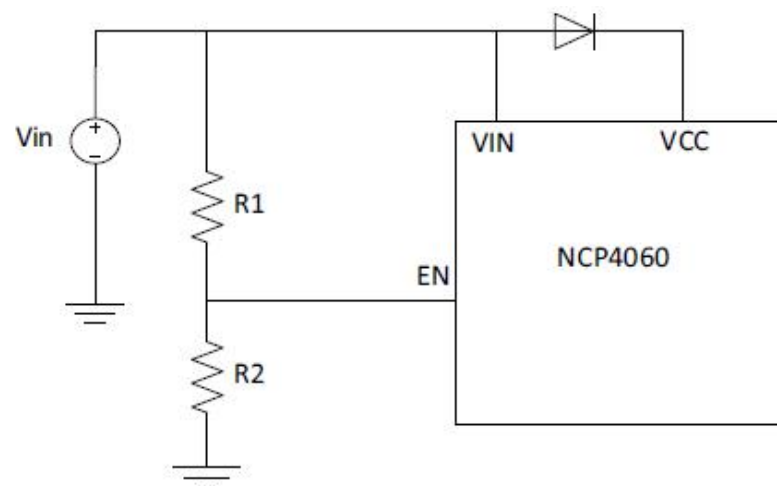
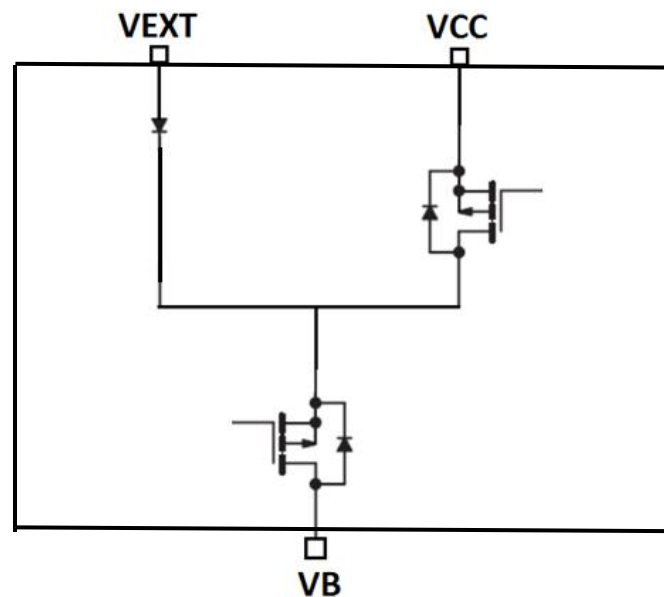
框图及引脚说明



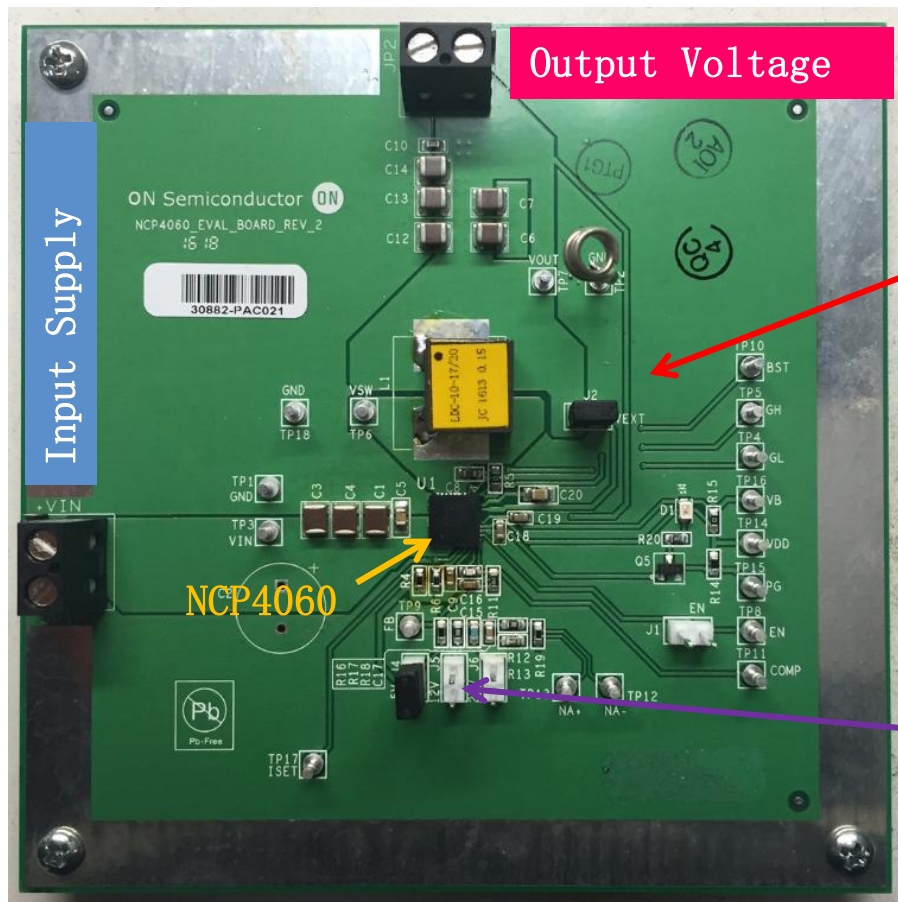
Pin No.	Symbol	Description
1	NC	No Connect
2	NC	No Connect
3-4	VSW	The VSW pin is connected to the drain of low-side MOSFET and the source of the high-side MOSFET.
5	PGND	Power ground reference and high-current return path for the low-side MOSFET and low-side MOSFET gate driver
6-7	VIN	The VIN pin is connected to the drain of high-side MOSFET. Decouple this pin to PGND by placing decoupling capacitors close to the IC
8	AGND	Analog ground
9	RT	A resistor from RT to AGND sets the switching frequency
10	ISET	A resistor from ISET pin to AGND sets the over-current protection (OCP) threshold
11	SS	A capacitor from SS pin to AGND allows the user to adjust the soft-start ramp time
12	FB	Connect FB to the center tap of external resistor divider to set the output voltage
13	COMP	Error Amplifier Output
14	EN	When used as EN pin, float or drive this pin to > 1.2V to enable the part; pull to ground to disable; for standby mode, drive this pin to a voltage between 0.8V & 1V. To implement VIN UVLO, and set the input voltage at which the part turns on, add a resistor divider from VIN to PGND, and connect the center-tap to EN.
15	PG	Power good indicator of the output voltage. Open-drain output. Connect PG to VDD with an external resistor
16	VDD	Analog input bias voltage. Connect to VB. Connect a 4.7uF ceramic capacitor from VDD to AGND
17	VB	5.25V LDO output and MOSFETs driver supply pin for NCP4060. Bypass VB by 4.7uF ceramic capacitor to AGND.
18	VEXT	Output voltage is connected to this pin to enable LDO switch-over scheme to reduce power consumption. If LDO switch-over scheme is not needed, tie VEXT to AGND.
19	VCC	VCC input voltage for the LDO. Connect to VIN.
20	BST	High-side MOSFET driver input supply, a bootstrap capacitor connection between the switch node and this pin

NCP4060 LDO开关电流

- VB由内部LDO产生，可通过VCC供电
- 为了减少损耗，也可以通过VEXT引脚连接到Vout
- 在预偏置时，VOUT有可能通过VCC反灌VIN，增加Vin和VCC之间的二极管可以防止这种情况发生



NCP4060 评估板

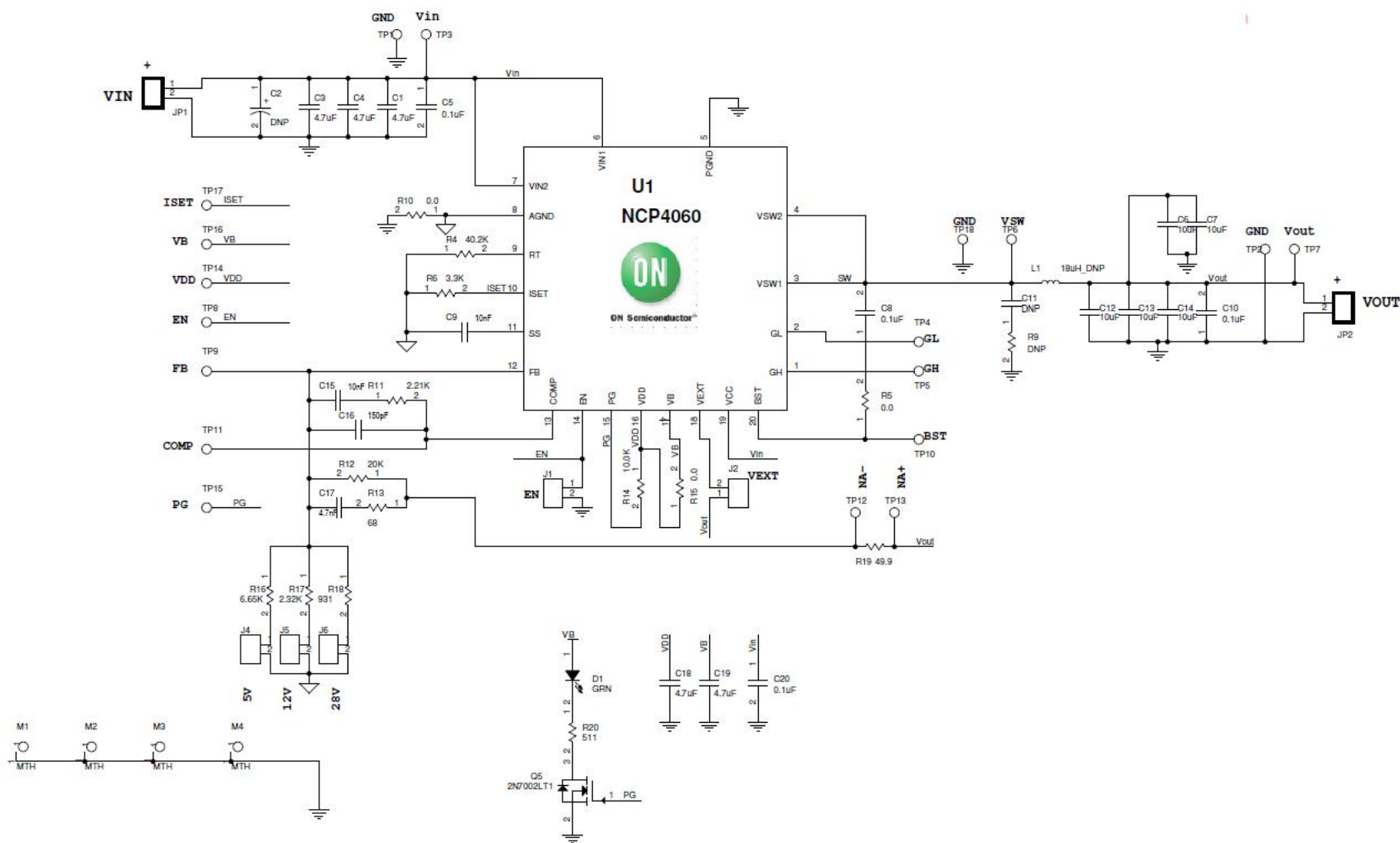


Jumper 连接Vout (>7.2V) 至 Vext pin. 若打开, Vin 会被选为内部LDO的输入

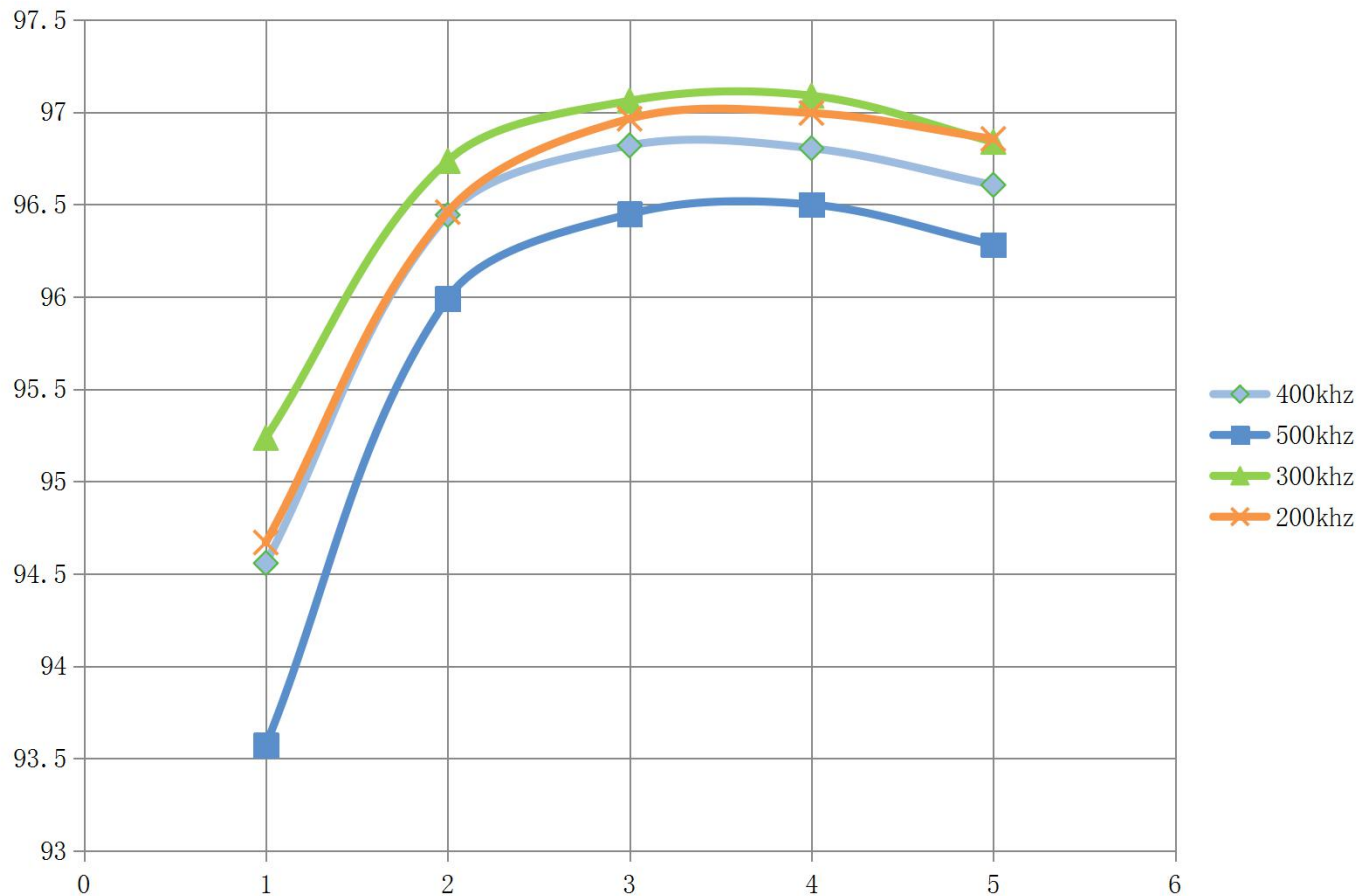
Jumpers 以选择输出电压 (5, 12 或 24V)

封装: 20Pin 6x6mm

评估板框图

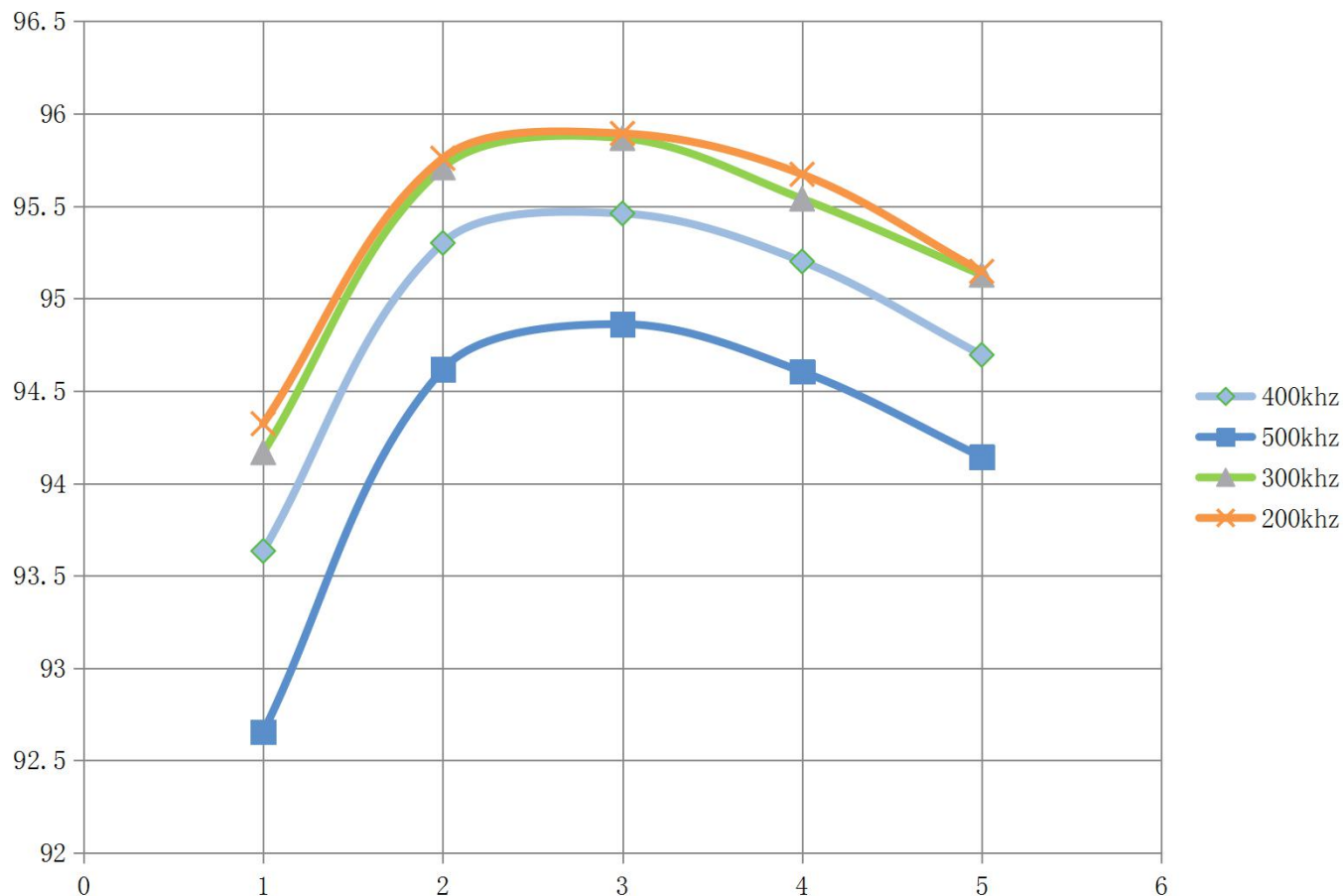


不同频率下的效率 ($V_{out}=24V$)



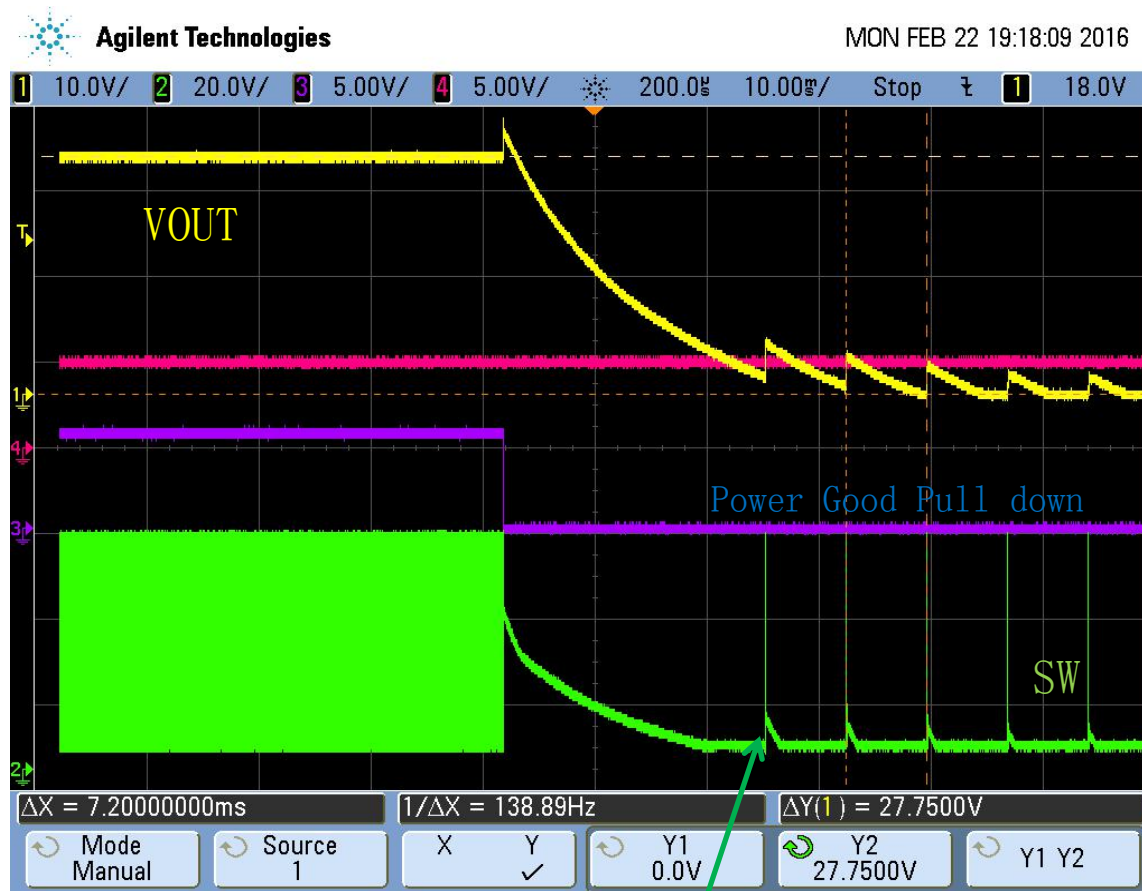
20z CU, $L=15\mu H$, $C_{out} = 5 \times 10\mu F$, $V_{out} = 24V$, $V_{in} = 48V$

不同频率下的效率 ($V_{out}=13.5V$)



20z CU, $L=15\mu H$, $C_{out} = 5 \times 10\mu F$, $V_{out} = 13.5V$, $V_{in} = 48V$

欠压保护



条件: FB Pin Pulled to GND

NCP4060 进入 Hiccup 模式

ENABLE

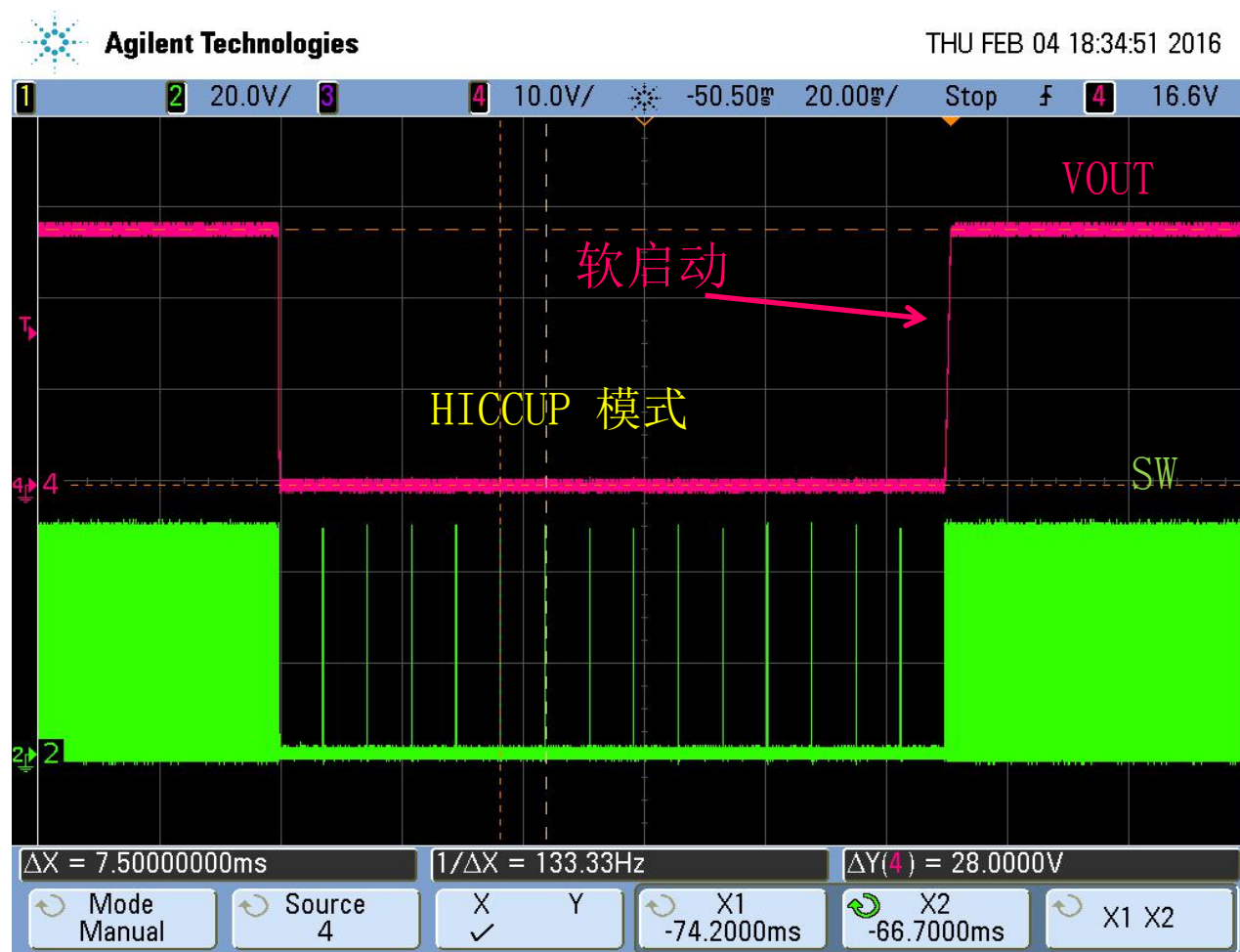


DISABLE



负载= 1A

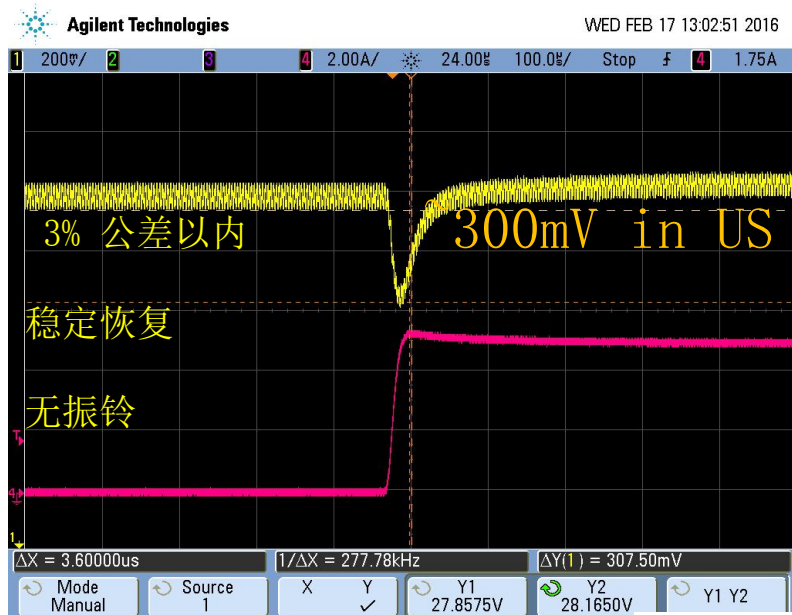
过流保护情况



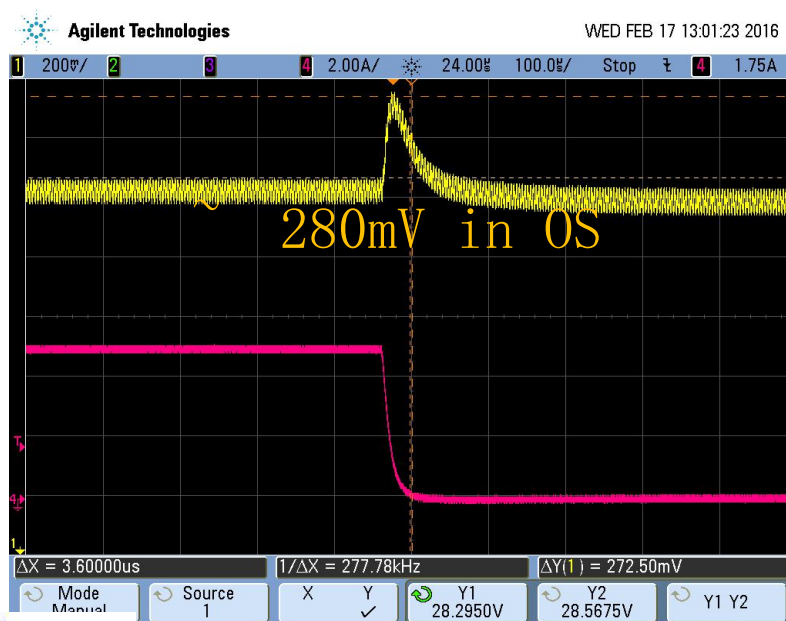
$$t_{\text{Hiccup}} = 4 * t_{\text{ss}}$$

动态表现

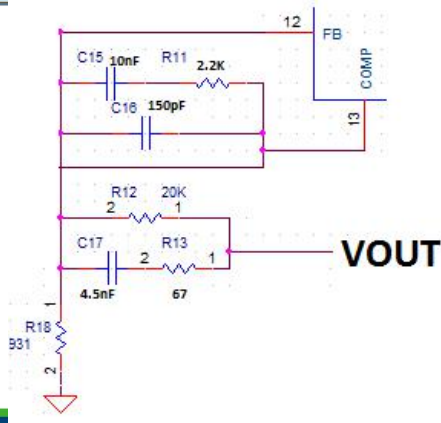
0 - 5A 瞬态负载@ 28Vout



负载上升

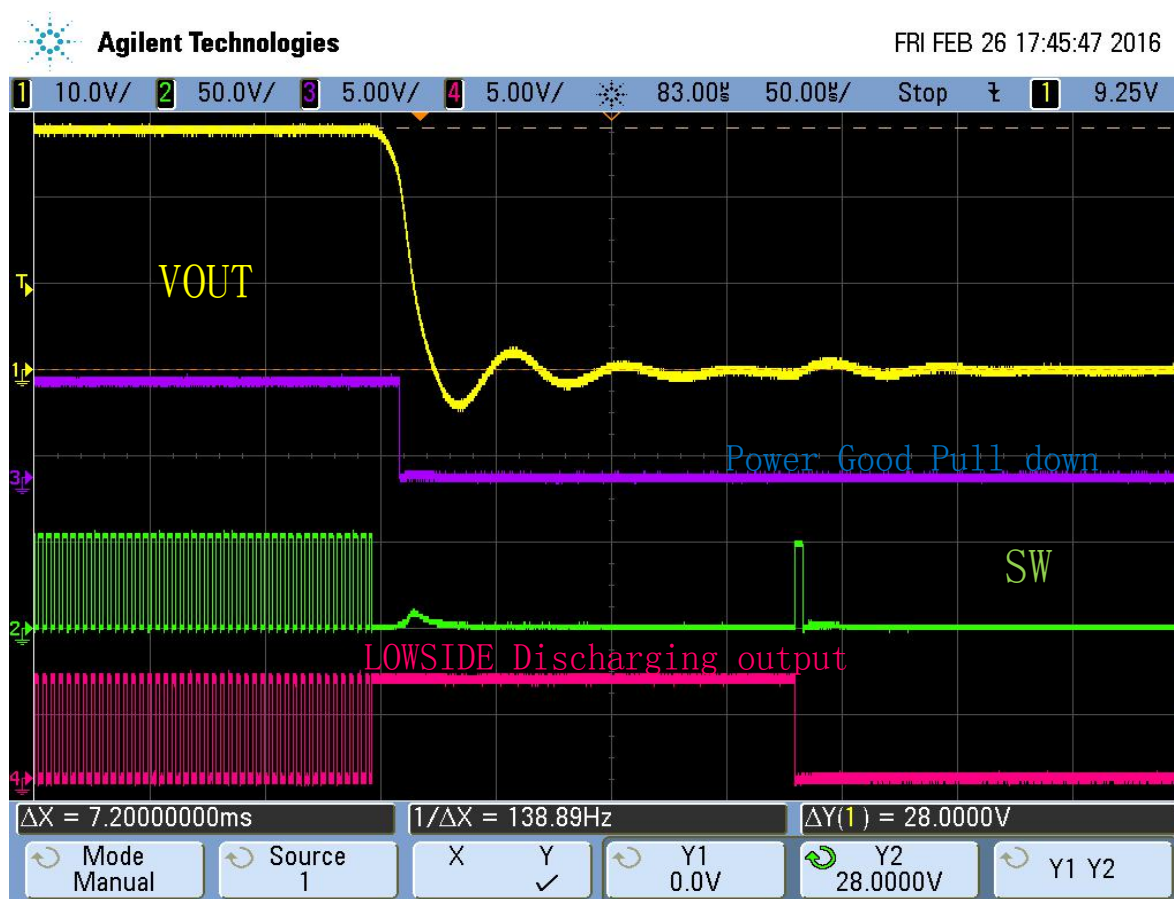


负载释放



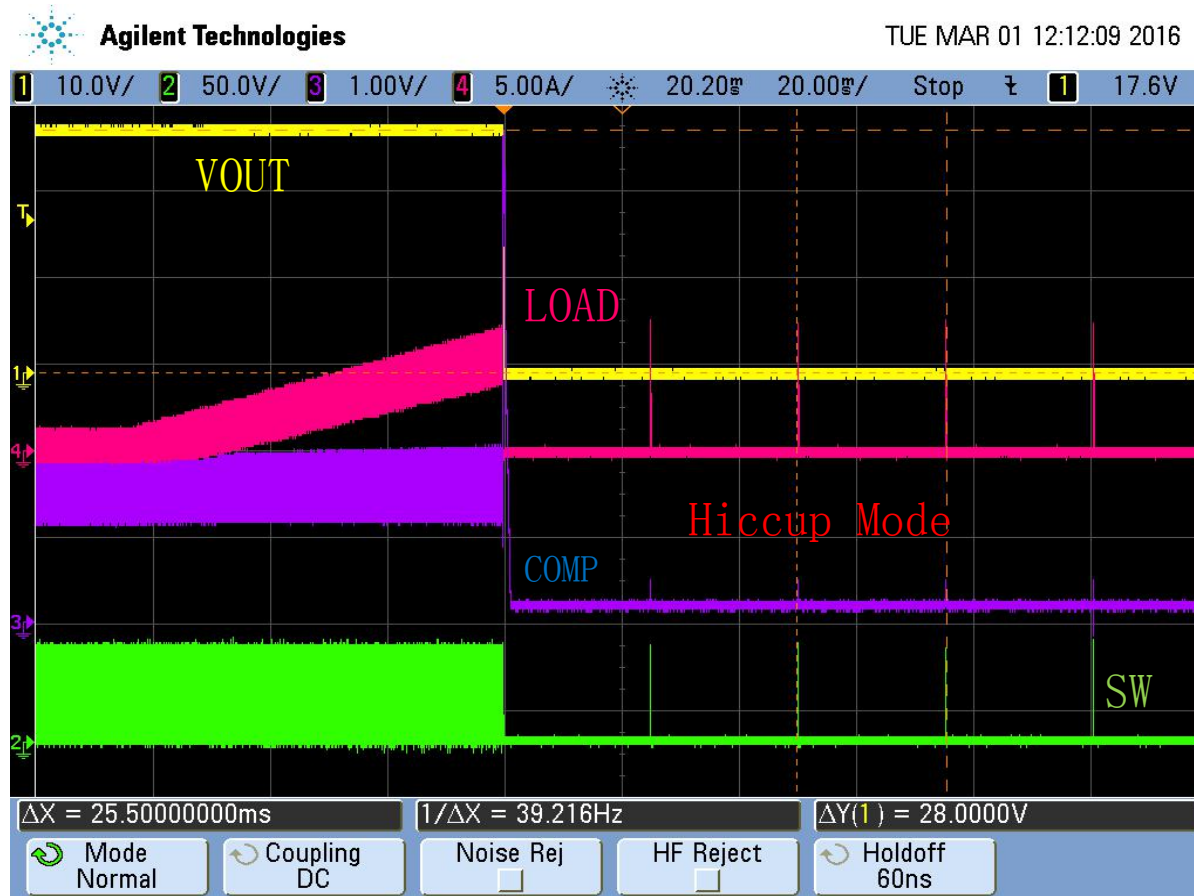
补偿网

过压保护情况



条件 : FB Pin Pulled High

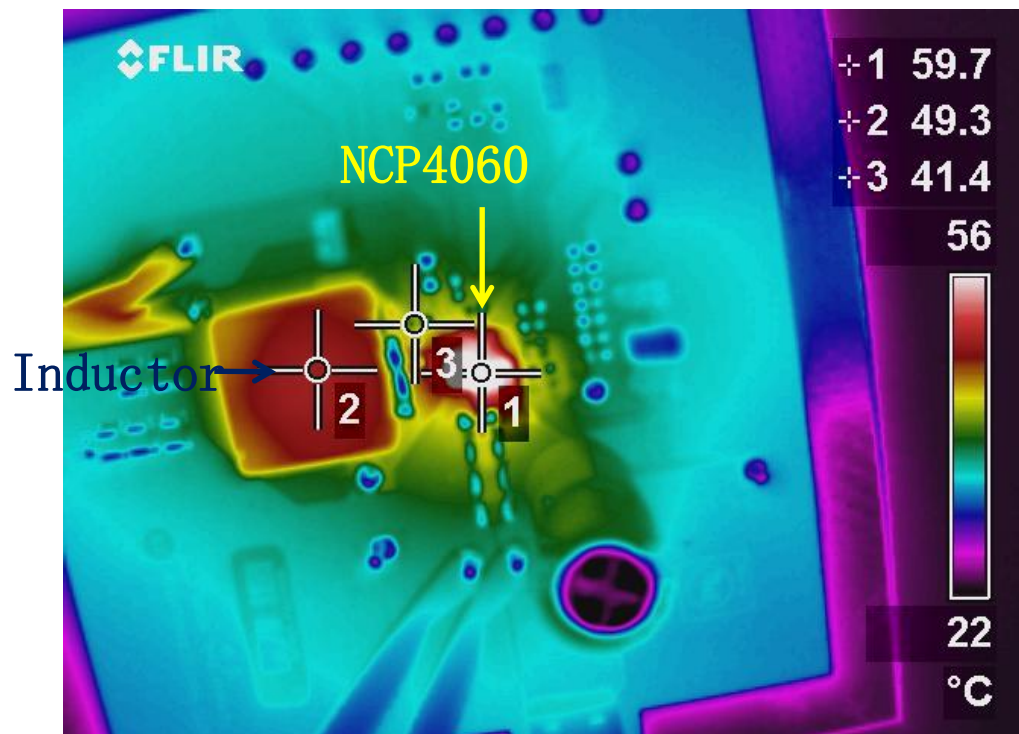
过流保护



NCP4060 于所有故障时使用 hiccup, 故障清除后回到软启动模式

NCP4060热性能

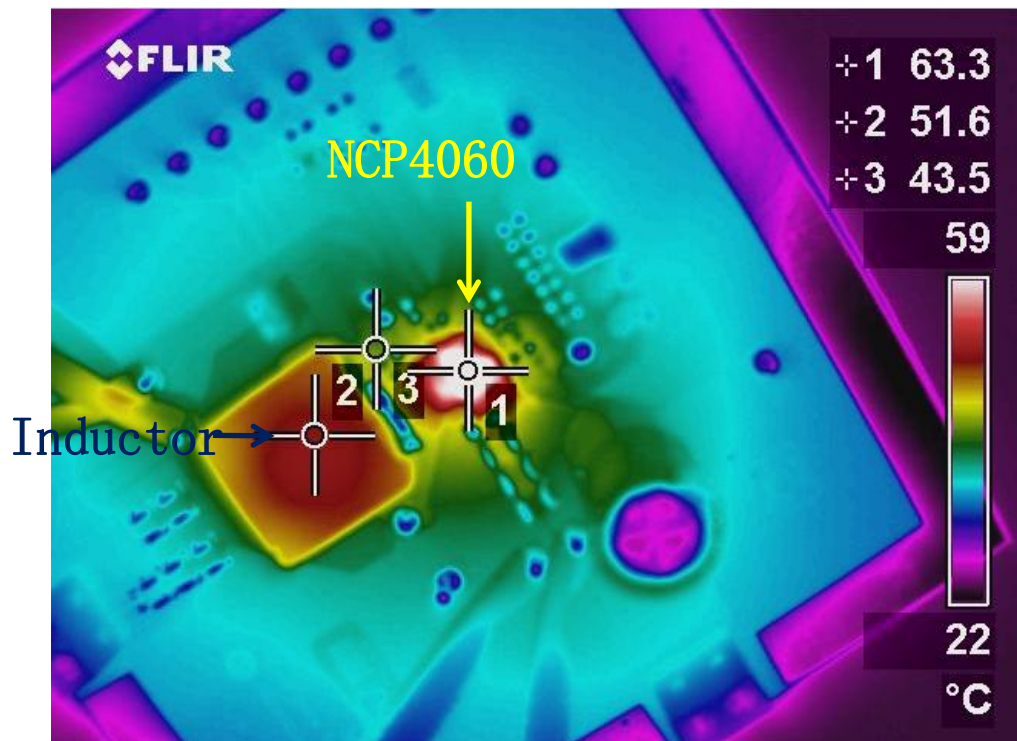
Load (A)	Junction (°C)
6A	60°C
5A	53°C
4A	48°C



20z Cu, $V_{OUT}=13.5V$, $F=280kHz$, $L=15\mu H$, $C_{out} = 5 \times 10\mu F$, Load = 6A

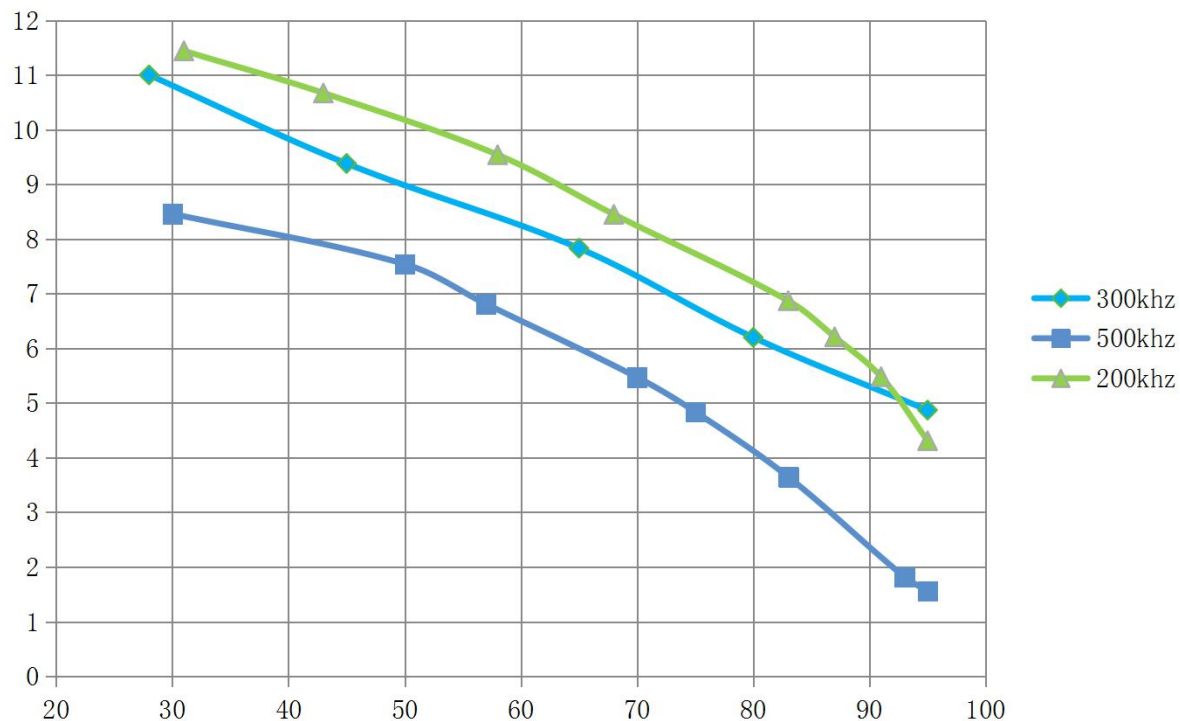
NCP4060热性能

Load (A)	Junction (C)
6A	63°C
5A	59°C
4A	54°C



20z Cu, $V_{OUT}=24V$, $F=280kHz$, $L=15\mu H$, $C_{out} = 5 \times 10\mu F$, Load = 6A

NCP4060的热降额曲线

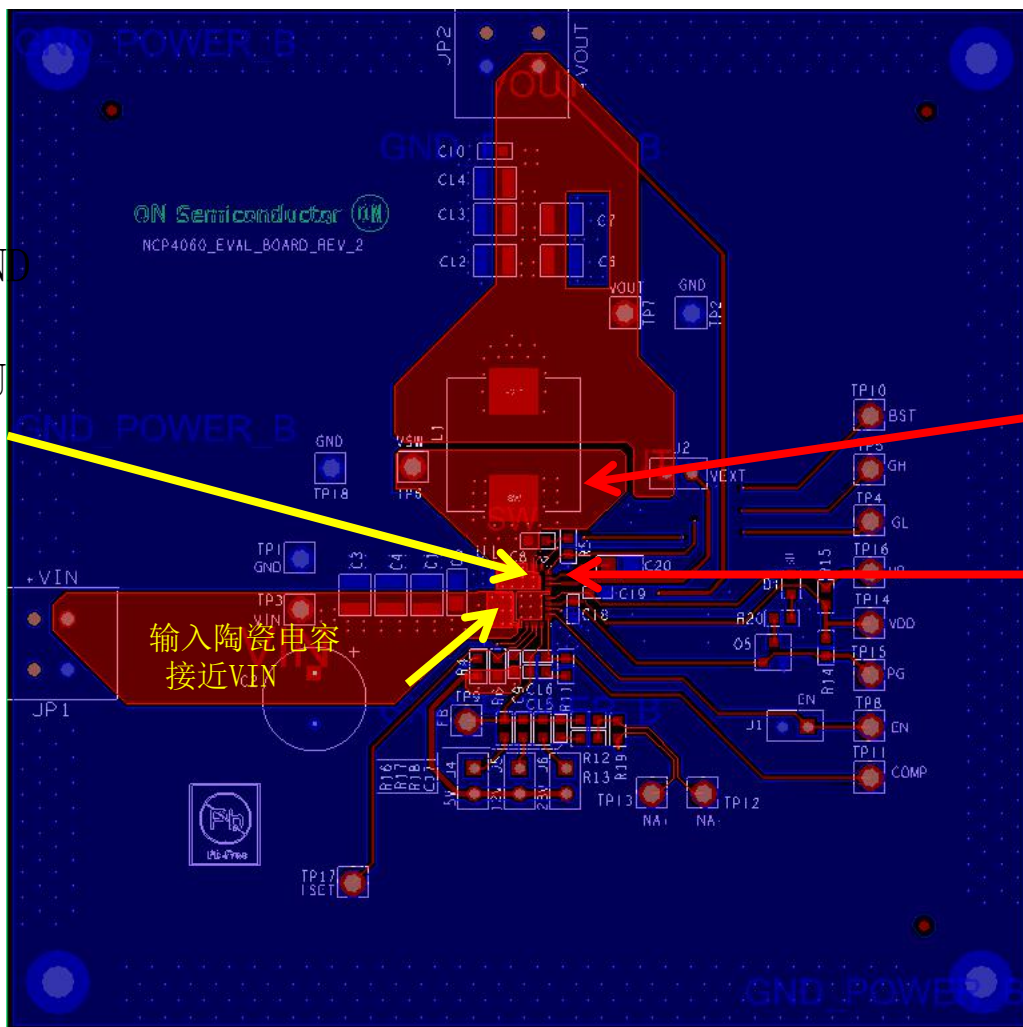


20z Cu, $V_{in}=48V$, $V_{out}=28V$, $L=22\mu H$, $C_{out}=5 \times 10\mu F$

于125°C时采集数据

布局建议

- *尽可能多的扩大GND面积
- * 每层使用 20%~30% 铜箔



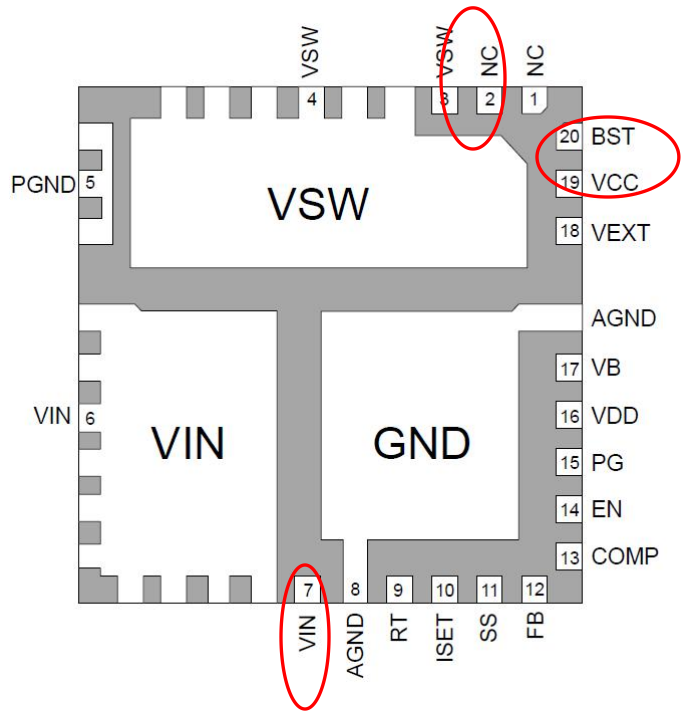
开关节点平面

建议至少5个 过孔,
使得SW热有效扩展
至内层

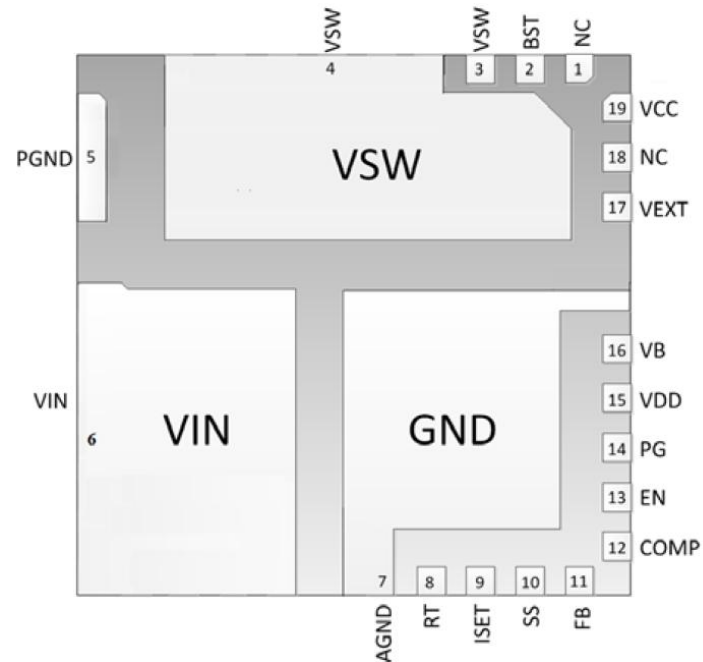
详细信息

- 提升热性能：在顶层和底层上浇铜，铜层的厚度极重要，建议使用2oz铜于所有层
- 使用VIN 及 VSW 外露盘散掉由高边及低边FET产生的热。扩大VIN及VSW的面积，尤其是接近硅的范围，外露盘有助散热
- 加上 过孔 连接顶层至里层及底层
- 避免信号连接打断VIN，VSW与GND
- 添加1uF 电容与R6并联，以过滤噪声
- 设定OCP阈值时使用12mohm为导通电阻。通过FET感应电流时排除键合线的寄生参数

NCP4060A – 改善隔离



NCP4060



NCP4060A

NCP4060A引脚介绍

Table 1. PIN DESCRIPTION

Pin No.	Symbol	Description
1	NC	No Connect
2	BST	High-side MOSFET driver input supply, a bootstrap capacitor connection between the switch node and this pin
3-4	VSW	The VSW pin is connected to the drain of the low-side MOSFET and the source of the high-side MOSFET.
5	PGND	Power ground reference
6	VIN	The VIN pin is connected to the drain of high-side MOSFET. Decouple this pin to PGND by placing decoupling capacitors close to the IC
7	AGND	Analog ground
8	RT	A resistor from RT to AGND sets the switching frequency
9	ISSET	A resistor from ISET pin to AGND sets the over-current protection (OCP) threshold
10	SS	A capacitor from SS pin to AGND allows the user to adjust the soft-start ramp time
11	FB	Connect FB to the center tap of external resistor divider to set the output voltage
12	COMP	Error Amplifier Output
13	EN	When used as EN pin, float or drive this pin to $> 1.2\text{ V}$ to enable the part; pull to ground to disable; for standby mode, drive this pin to a voltage between 0.8 V & 1 V . To implement VIN UVLO, and set the input voltage at which the part turns on, add a resistor divider from VIN to PGND, and connect the center-tap to EN.
14	PG	Power good indicator of the output voltage. Open-drain output. Connect PG to VDD with an external resistor
15	VDD	Analog input bias voltage. Connect to VB. Connect a $4.7\text{ }\mu\text{F}$ ceramic capacitor from VDD to AGND
16	VB	5.25 V LDO output and MOSFETs driver supply pin for NCP4060A. Bypass VB by $4.7\text{ }\mu\text{F}$ ceramic capacitor to AGND.
17	VEXT	Output voltage is connected to this pin to enable LDO switch-over scheme to reduce power consumption. If LDO switch-over scheme is not needed, tie VEXT to AGND.
18	NC	No Connect
19	VCC	VCC input voltage for the LDO. Connect to VIN.

总结

- NCP4060是高度集成的高压POL，用于电信及工业应用
- 80V 输入电压及高达 6A 电流，28V 输出
- 高能效及极佳的热表现
- 简单外部电路，易于使用

更多产品信息

有关安森美半导体NCP4060的更多信息，请访问网站：

www.onsemi.cn

详细信息请联系您当地的安森美半导体销售代表或授权代理商。

www.onsemi.cn/PowerSolutions/locateSalesSupport.do

关注“安森美半导体”官方微信平台

扫描二维码 点击关注

